(ISO9001:2015)

MODEL NO. : HGO1286427-P-F

MANUFACTURER : TSINGTEK DISPLAY CO.,LTD

REVISION : A

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| Rev. NO. | Date | CONTENTS | REMARKS |
|---|---|---|---|
| A | Aug.17, 2020 | First Release | |
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# CONTENTS

# 1. BASIC SPECIFICATION

## 1.1 DISPLAY SPECIFICATION

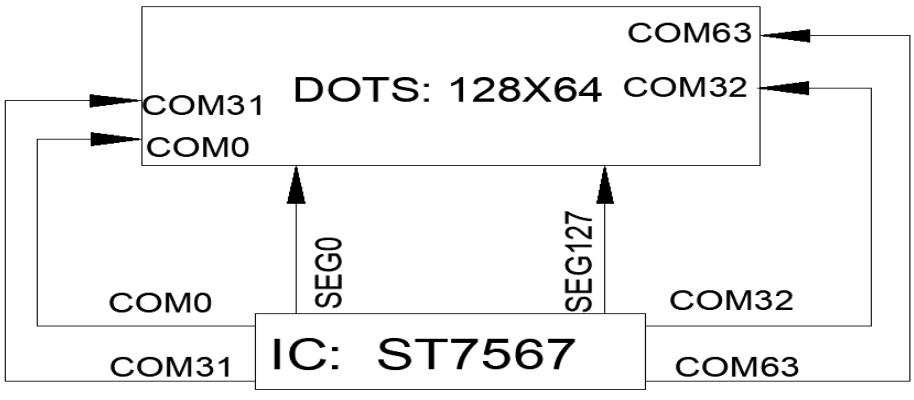
| ITEM | SPECIFICATION |
|---|---|
| DISPLAY TYPE | FSTN/POSITIVE/TRANSFLECTIVE |
| INPUT DATA | 8-BIT 6800 PARALLEL 、8-BIT 8080 PARALLEL 、4-WIRE SERIAL |
| DUTY | 1/64 DUTY |
| VIEW ANGLE | 6 O'CLOCK |
| CONTROLLER | ST7567 or Equivalent |
| OPERATING TEMPERATURE | -30℃ ~ 80℃ |
| STORAGE TEMPERATURE | -40℃ ~ 80℃ |

## 1.2 MECHANICAL SPECIFICATION

| ITEM | SPECIFICATION | UNIT |
|---|---|---|
| OUTLINE DIMENSION | 40.0(W)×31.6 (H)×2.1MAX.(T) | mm |
| VIEWING AREA | 37.0(W)×22.5(H) | mm |
| ACTIVE AREA | 33.26(W)×18.54(H) | mm |
| DOTS | 128Dots×64Dots | --- |
| DOT PITCH | 0.26(W)×0.29(H) | mm |
| DOT SIZE | 0.24(W)×0.27(H) | mm |

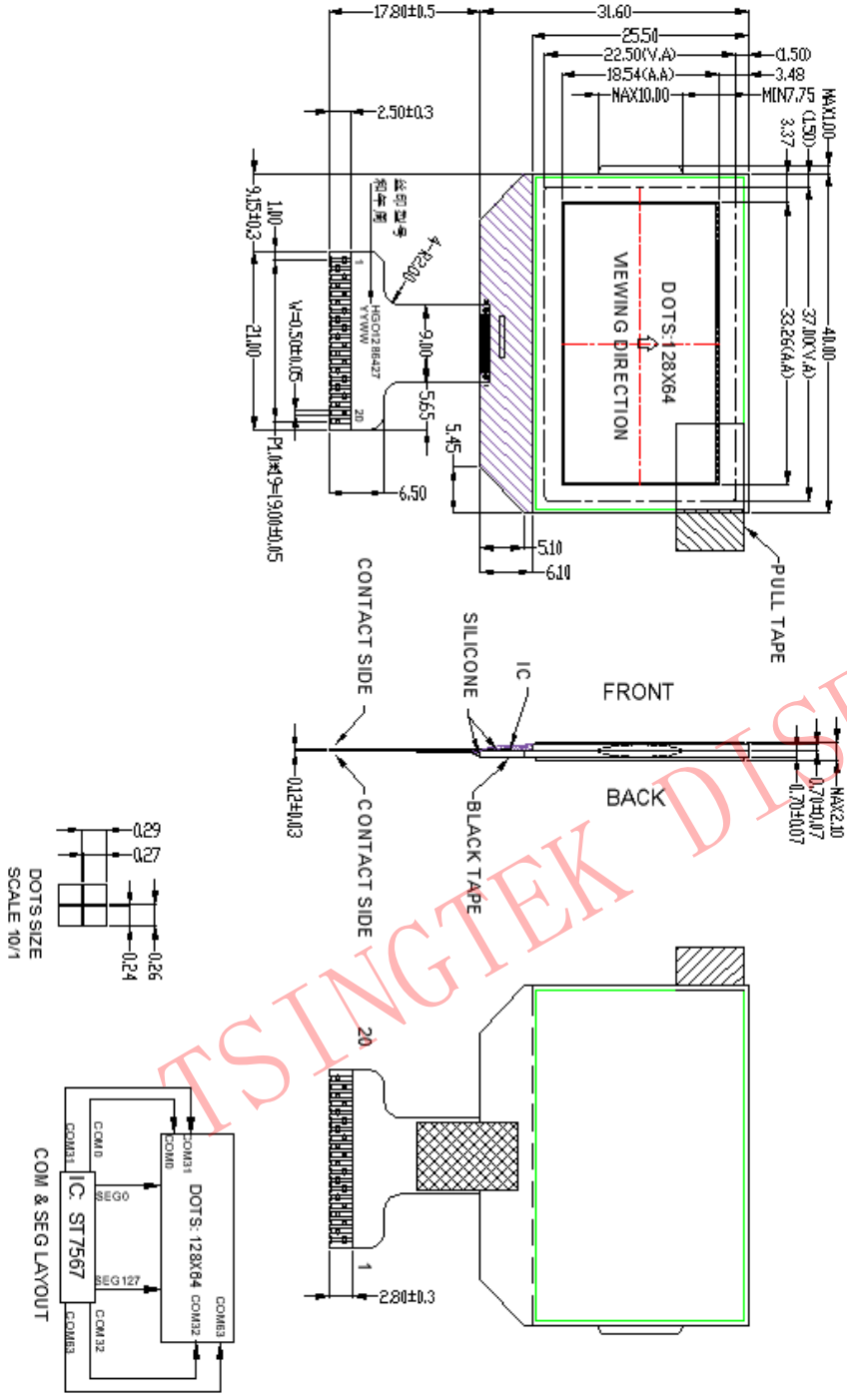


## 1.3 BLOCK DIAGRAM




COM & SEG LAYOUT

# 1.4 DIMENSIONAL OUTLINE




| PIN Definition | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 |
| PSB | C86 | VG | XV0 | V0 | VSS | VDD | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | /RD | /RW | A0 | RSTB | CSB |

# 1.5 TERMINAL FUNCTIONS

<table>
<tr><th>Pin No.</th><th>Symbol</th><th>Signal Description</th></tr>
<tr><td>1</td><td>PSB</td><td>PSB selects the interface type: Serial or Parallel.</td></tr>
<tr><td>2</td><td>C86</td><td>C86 selects the microprocessor type in parallel interface mode.</td></tr>
<tr><td>3</td><td>VG</td><td>VG is the LCD driving voltage for segment circuits.</td></tr>
<tr><td>4</td><td>XV0</td><td>XV0 is the LCD driving voltage for common circuits at positive frame.</td></tr>
<tr><td>5</td><td>V0</td><td>V0 is the LCD driving voltage for common circuits at negative frame.</td></tr>
<tr><td>6</td><td>VSS</td><td>ground.</td></tr>
<tr><td>7</td><td>VDD</td><td>Power Supply</td></tr>
<tr><td>8~15</td><td>D7~D0</td><td>When using 8-bit parallel interface: (6800 or 8080 mode)<br>8-bit bi-directional data bus. Connect to the data bus of 8-bit microprocessor. When CSB is non-active (CSB="H"), D[7:0] pins are high impedance.<br>When using serial interface: 4-LINE<br>D7=SDA: Serial data input.<br>D6=SCL: Serial clock input.<br>D[5:0] are not used and should connect to "H" by VDD.<br>When CSB is non-active (CSB="H"), D[7:0] pins are high impedance.</td></tr>
<tr><td>16</td><td>/RD</td><td>Read/Write execution control pin. When P/S is "H",
<table>
<tr><th>C86</th><th>MPU Type</th><th>ERD</th><th>Description</th></tr>
<tr><td>H</td><td>6800 series</td><td>E</td><td>Read/Write control input pin.<br>R/W="H": When E is "H", D[7:0] are in output mode.<br>R/W="L": Signals on D[7:0] are latched at the falling edge of E signal.</td></tr>
<tr><td>L</td><td>8080 series</td><td>/RD</td><td>Read enable input pin.<br>When /RD is "L", D[7:0] are in output mode.</td></tr>
</table>
/RD is not used in serial interface and should fix to "H" by VDD.</td></tr>
<tr><td>17</td><td>/RW</td><td>Read/Write execution control pin. When PSB is "H",
<table>
<tr><th>C86</th><th>MPU Type</th><th>RWR</th><th>Description</th></tr>
<tr><td>H</td><td>6800 series</td><td>R/W</td><td>Read/Write control input pin.<br>R/W="H": read.<br>R/W="L": write.</td></tr>
<tr><td>L</td><td>8080 series</td><td>/WR</td><td>Write enable input pin.<br>Signals on D[7:0] will be latched at the rising edge of /WR signal.</td></tr>
</table>
/RW is not used in serial interface and should fix to "H" by VDD.</td></tr>
<tr><td>18</td><td>A0</td><td>It determines whether the access is related to data or command.<br>A0="H" : Indicates that signals on D[7:0] are display data.<br>A0="L" : Indicates that signals on D[7:0] are command.</td></tr>
<tr><td>19</td><td>RSTB</td><td>Hardware reset input pin. When RSTB is "L", internal initialization is executed and the internal registers will be initialized.</td></tr>
<tr><td>20</td><td>CSB</td><td>Chip select input pin. Interface access is enabled when CSB is "L". When CSB is non-active (CSB="H"), D[7:0] pins are high impedance.</td></tr>
</table>

# 2. ABSOLUTE MAXIMUM RATINGS

| Item | Symbol | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| Power Supply Voltage | $V_{DD}$ | — | -0.3 | +3.6 | V |
| LCD Power Supply Voltage | V0-XV0 | — | -0.3 | +16 | V |
| LCD Power Supply Voltage | VG | | -0.3 | +3.6 | V |
| Operating Temperature | $T_{OP}$ | — | -30 | 80 | ℃ |
| Storage Temperature | $T_{ST}$ | — | -40 | 80 | ℃ |
| Storage Humidity | $H_D$ | Ta＜60 ℃ | - | 90 | %RH |

# 3.ELECTRICAL CHARACTERISTICS

## 3.1 ELECTRICAL CHARACTERISTICS

$V_{DD}$=3.0 V ±5%，$V_{SS}$=0V，Ta = 25℃

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Operating Voltage | $V_{DD}$ | - | 2.85 | 3.0 | 3.15 | V |
| Input High-level Voltage | $V_{IHC}$ | - | 0.7$V_{DD}$ | - | $V_{DD}$ | V |
| Input Low-level Voltage | $V_{ILC}$ | - | $V_{SS}$ | - | 0.3$V_{DD}$ | V |
| Output High-level Voltage | $V_{OHC}$ | - | 0.8$V_{DD}$ | - | $V_{DD}$ | V |
| Output Low-level Voltage | $V_{OLC}$ | - | $V_{SS}$ | - | 0.2$V_{DD}$ | V |
| LCD Supply Power | $V_{LCD}$ | - | 10.8 | 11.0 | 11.2 | V |
| Supply Current | $I_{DD}$ | $V_{DD}$=3.0V,Vop=11.0V，Pattern= Vertical display | - | 0.27 | 0.40 | mA |



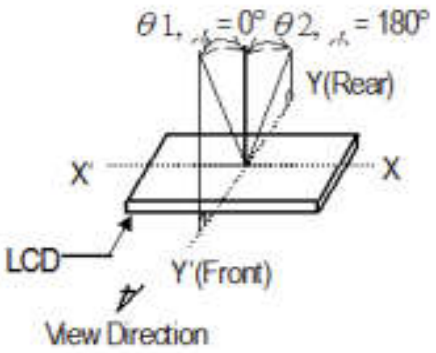
## 3.2 LED BACKLIGHT SPECIFICATION

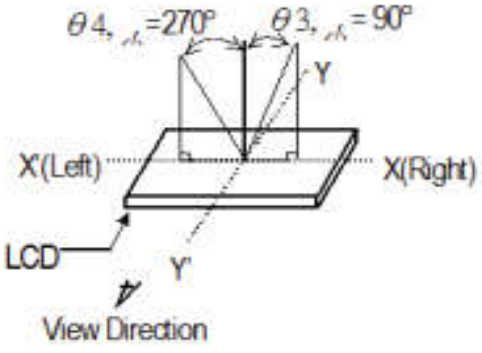
LCD Panel：1/65Duty，1/9Bias，$V_{LCD}$=11.0V，Ta=25℃

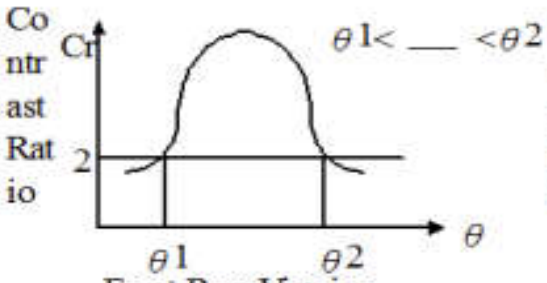
| Item | | Symbol | Conditions | Min. | Typ. | Max. | Unit | Reference |
|---|---|---|---|---|---|---|---|---|
| Response Time | | Ton | C≥2.0 | - | 150 | 250 | ms | Note3 |
| | | Toff | | - | 180 | 300 | | |
| Viewing angle range | =0(6H) | Y' | | 30 | 40 | - | Deg. | Note 1 |
| | =90(3H) | X | | 20 | 35 | - | | |
| | =180(12H) | Y | | 10 | 20 | - | | |
| | =270(9H) | X' | | 25 | 35 | - | | |
| Contrast Ratio | | C | θ = 0° | 3 | 6 | - | - | Note 2 |

Note 1

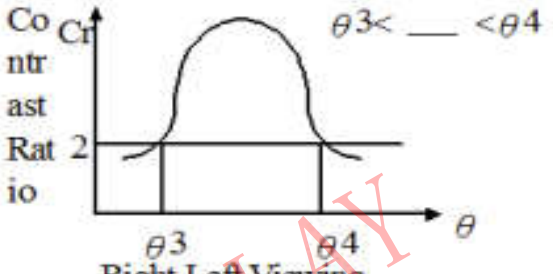
Definition of viewing angle




Front-Rear Viewing Angle

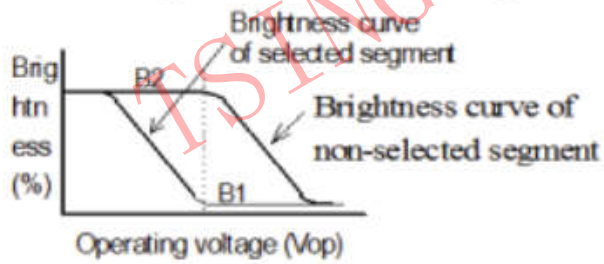



Right-Left Viewing Angle

Note 2

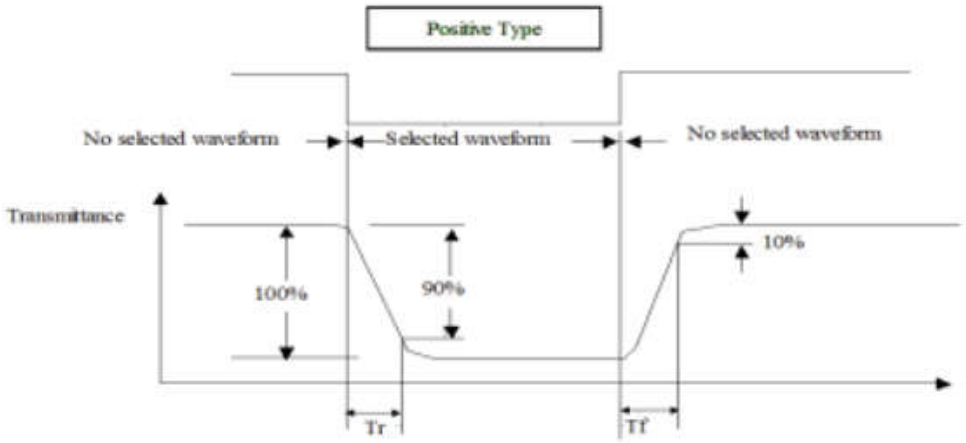
Definition of contrast

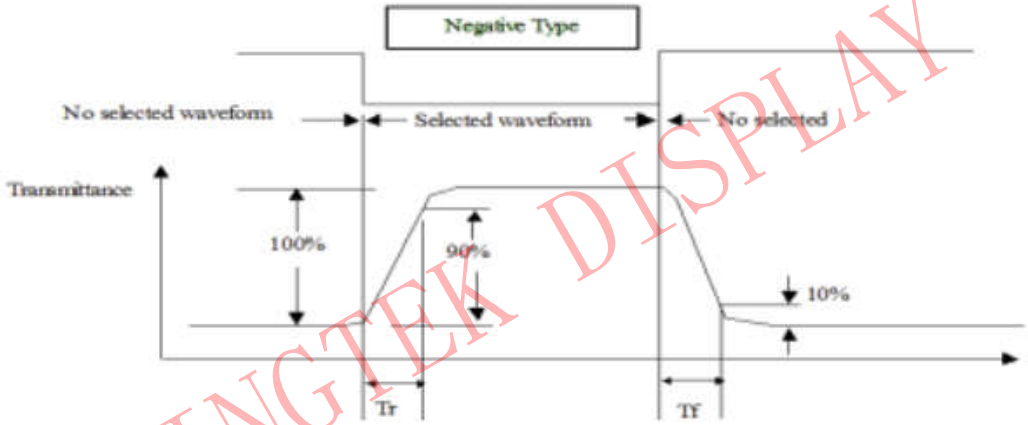
$$C.R = \frac{\text{RATIO}\ \text{Brightness of non-selected segment (B2)}}{\text{Brightness of selected segment}}$$



Note 3

Definition of response time

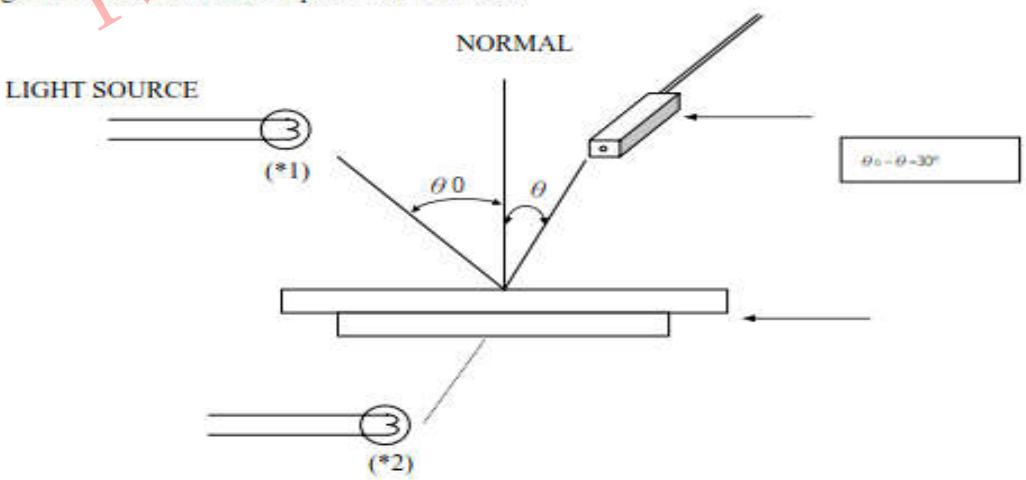





Note 4

Measuring Instruments For Electro-optical Characteristics




*1.Light source position for measuring the reflective type of LCD panel

*2.Light source position for measuring the transflective / transmissive types of LCD panel

# 4.TIMING CHARACTERISTICS

## Microprocessor Interface

### Chip Select Input

CSB pin is used for chip selection. When CSB is "L", the microprocessor interface is enabled and ST7567 can interface with an MPU. When CSB is "H", the inputs of A0, ERD and RWR with any combination will be ignored and D[7:0] are high impedance. In 4-Line serial interface, the internal shift register and serial counter are reset when CSB is "H".

### Interface Selection

The interface selection is controlled by C86 and PSB pins. The selection for parallel or serial interface is shown in Table 1.

**Table 1. Parallel/Serial Interface Mode**

| PSB | C86 | CSB | A0 | ERD | RWR | D[7:0] | MPU Interface |
|---|---|---|---|---|---|---|---|
| "H" | "H" | CSB | A0 | E | R/W | D[7:0] | 6800-series parallel interface |
| "H" | "L" | | | /RD | /WR | | 8080-series parallel interface |
| "L" | "X" | | | --- | --- | Refer to serial interface. | 4-Line SPI interface |

* The un-used pins are marked as "---" and should be fixed to "H" by VDD1 or VDDH.

### Parallel Interface

When PSB= "H", the 8-bit bi-directional parallel interface is enabled and the type of MPU is selected by "C86" pin as shown in Table 2. The data transfer type is determined by signals on A0, ERD and RWR as shown in Table 3.

**Table 2. Microprocessor Selection for Parallel Interface**

| PSB | C86 | CSB | A0 | ERD | RWR | D[7:0] | MPU Interface |
|---|---|---|---|---|---|---|---|
| "H" | "H" | CSB | A0 | E | R/W | D[7:0] | 6800-series parallel interface |
| "H" | "L" | | | /RD | /WR | | 8080-series parallel interface |

**Table 3. Parallel Data Transfer Type**

| Common Pins | | 6800-Series | | 8080-Series | | Description |
|---|---|---|---|---|---|---|
| CSB | A0 | E (ERD) | R/W (RWR) | /RD (ERD) | /WR (RWR) | |
| "L" | "H" | "H" | "H" | "L" | "H" | Display data read out |
| | "H" | "H" | "L" | "H" | "L" | Display data write |
| | "L" | "H" | "H" | "L" | "H" | Internal status read |
| | "L" | "H" | "L" | "H" | "L" | Writes to internal register (instruction) |

### Setting Serial Interface

| Serial Mode | PSB | C86 | CSB | A0 | ERD | RWR | D[7:0] |
|---|---|---|---|---|---|---|---|
| 4-Line SPI interface | "L" | X | CSB | A0 | --- | --- | SDA, SCLK, ---, ---, ---, ---, ---, --- |

* The un-used pins are marked as "---" and should be fixed to "H" by VDD1 or VDDH.

* C86 is marked as "X" and can be fixed to "H" or "L".

Note:

1. The option setting to be "H" should connect to VDD1 or VDDH.
2. The option setting to be "L" should connect to VSS1 or VSSL.

**4-line SPI interface (PSB="L", C86="H" or "L")**

When ST7567 is active (CSB="L"), serial data (SDA) and serial clock (SCLK) inputs are enabled. When ST7567 is not active (CSB="H"), the internal 8-bit shift register and 3-bit counter are reset. Serial data on SDA is latched at the rising edge of serial clock on SCLK. After the 8th serial clock, the serial data will be processed to be 8-bit parallel data. The address selection pin (A0), which is latched at the 8th clock, indicates the 8-bit parallel data is display data or instruction. The 8-bit parallel data will be display data when A0 is "H" and will be instruction when A0 is "L". The read feature is not available in this mode. The DDRAM column address pointer will be increased by one automatically after each byte of DDRAM access. Please note that the SCLK signal quality is very important and external noise maybe causes unexpected data/instruction latch.

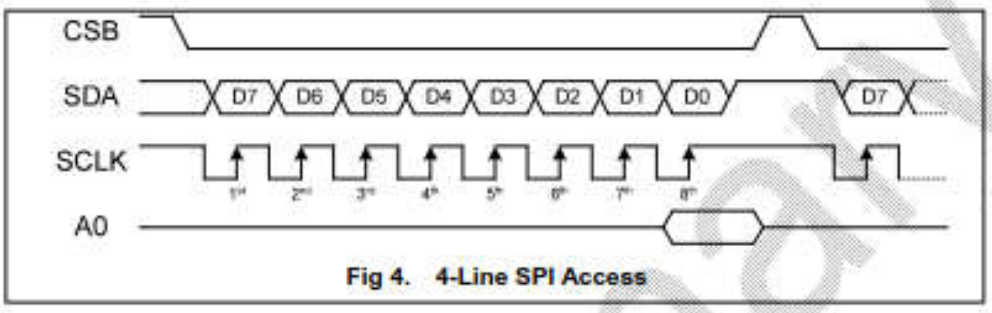



**Fig 4. 4-Line SPI Access**

Note:

- Some MPU will set the interface to be Hi-Z (high impedance) mode when power saving mode or after hardware reset. This is not allowed when the VDD1of ST7567 is turned ON. Because the floating input (especially for those control pins such as CSB, RSTB, RWR or ERD...) maybe cause abnormal latch and cause abnormal display.

## Display Data RAM (DDRAM)

ST7567 is built-in a RAM with 65X132 bit capacity which stores the display data. The display data RAM (DDRAM) store the dot data of the LCD. It is an addressable array with 132 columns by 65 rows (8-page with 8-bit and 1-page with 1-bit). The X-address is directly related to the column output number. Each pixel can be selected when the page and column addresses are specified (please refer to Fig 7 for detailed illustration). The rows are divided into: 8 pages (Page-0 ~ Page-7) each with 8 lines (for COM0~63) and Page-8 with only 1 line (COMS, for icon). The display data (D7~D0) corresponds to the LCD common-line direction and D0 is on top. All pages can be accessed through D[7:0] directly except icon page. Icon RAM uses only 1-bit of data bus (D0). Refer to Fig 8 for detailed illustration. The microprocessor can write to and read from (only Parallel interfaces) DDRAM by the I/O buffer. Since the LCD controller operates independently, data can be written into DDRAM at the same time as data is being displayed without causing the LCD flicker or data-conflict.

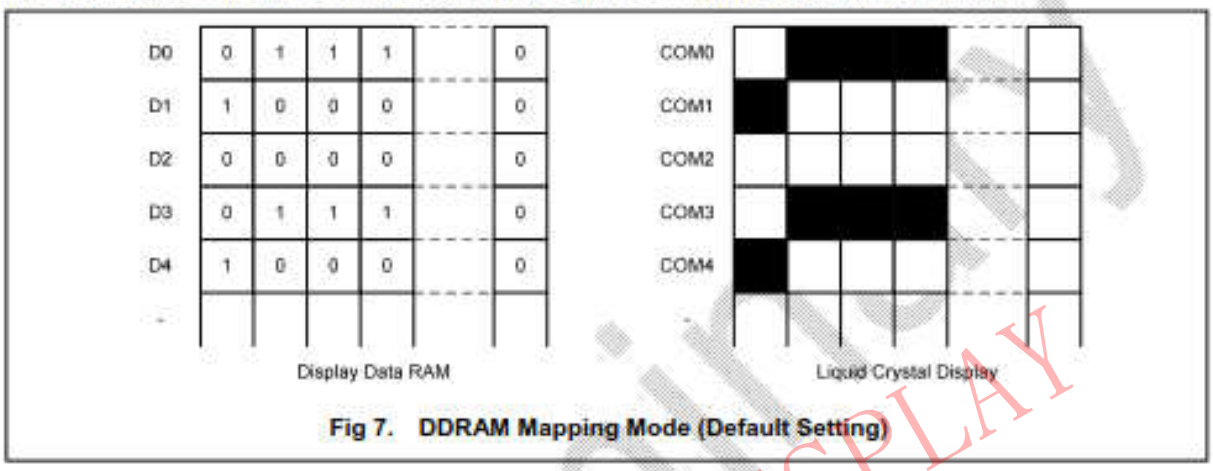



**Fig 7. DDRAM Mapping Mode (Default Setting)**

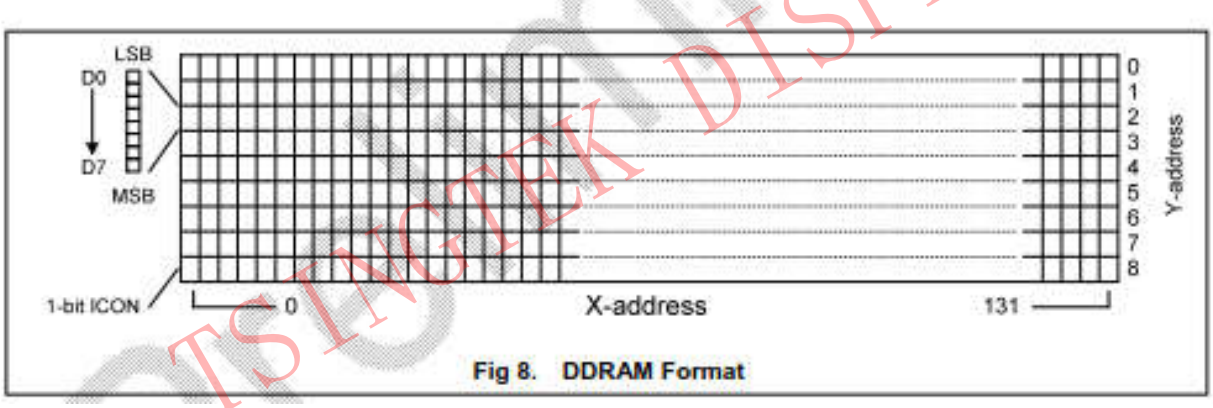



**Fig 8. DDRAM Format**

### Addressing

Data is downloaded into the Display Data RAM matrix in ST7567 as byte-format. The Display Data RAM has a matrix of 65 by 132 bits. The address ranges are: X=0~131 (column address), Y=0~8 (page address). Addresses outside these ranges are not allowed.

#### Page Address Circuit

This circuit provides the page address of DDRAM. It incorporates 4-bit Page Address Register which can be modified by the "Page Address Set" instruction only. The Page Address must be set before accessing DDRAM content. Page Address "8" is a special RAM area for the icons with only one valid bit: D0.

#### Column Address Circuit

The column address of DDRAM is specified by the Column Address Set command. The column address is increased (+1) after each display data access (read/write). This allows MPU accessing DDRAM content continuously. This feature stops at the end of each page (Column Address "83h") because the Column Address and Page Address circuits are independent. For example, both Page Address and Column Address should be assigned for changing the DDRAM pointer from (Page-0, Column-83h) to (Page-1, Column-0).

Furthermore, Register MX and MY makes it possible to invert the relationship between the DDRAM and the outputs (COM/SEG). It is necessary to rewrite the display data into DDRAM after changing MX setting.

The relation between DDRAM and outputs with different MX or MY setting is shown below.


Fig 9. DDRAM and Output Map (COM/SEG)

### Line Address Circuit

The Line Address Circuit incorporates a counter and a Line Address register which is changed only by the "Display Start Line Set" instruction. This circuit assigns DDRAM a Line Address corresponding to the first display line (COM0). Therefore, by setting Line Address repeatedly, ST7567 can realize the screen scrolling without changing the contents of DDRAM as shown in Fig 10. The last common is always the COMS (common output for the icons). That means the icons will never scroll with the general display data.

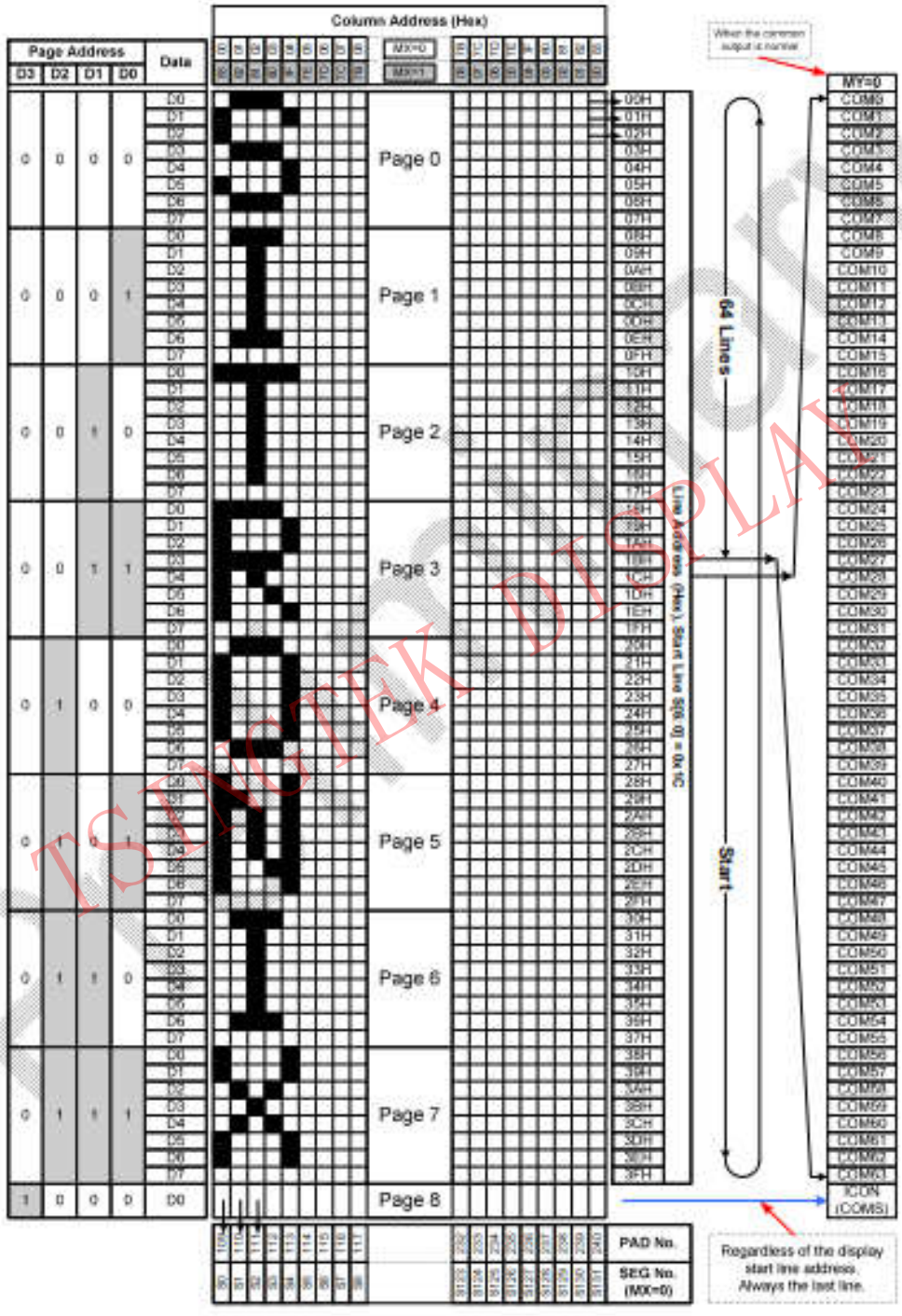
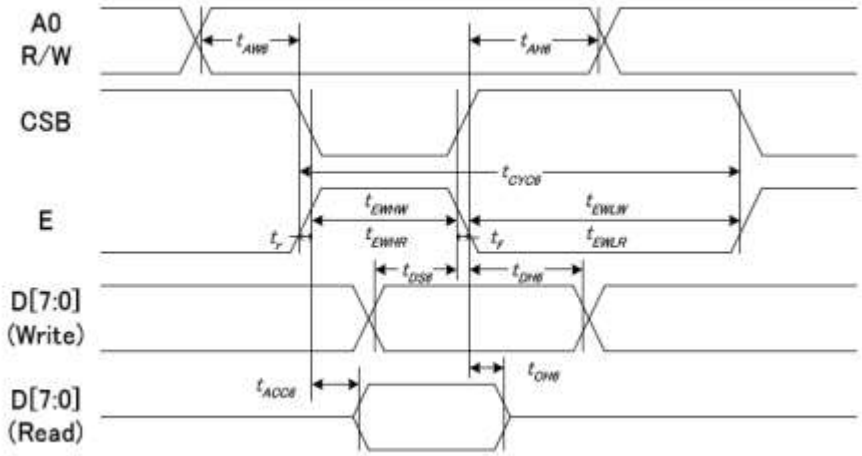



**Fig 10. Start Line Function**

**System Bus Timing for 6800 Series MPU**




(VDD1 = 3.3V , Ta =25°C)

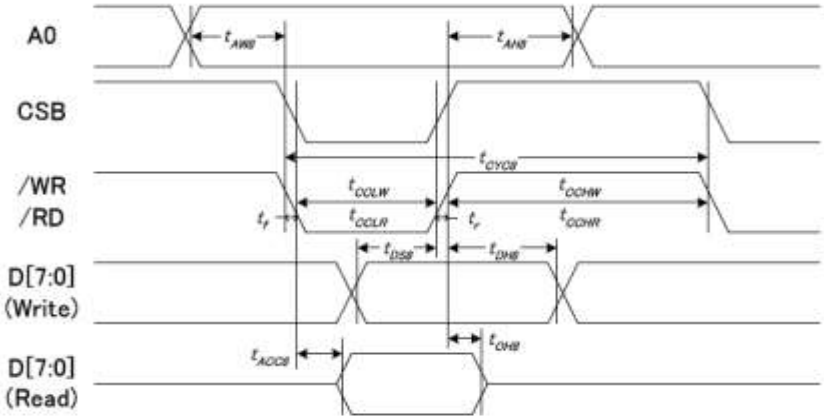
| Item | Signal | Symbol | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| Address setup time | A0 | tAW6 | | 0 | — | ns |
| Address hold time | | tAH6 | | 10 | — | |
| System cycle time | E | tCYC6 | | 240 | — | |
| Enable L pulse width (WRITE) | | tEWLW | | 80 | — | |
| Enable H pulse width (WRITE) | | tEWHW | | 80 | — | |
| Enable L pulse width (READ) | | tEWLR | | 80 | — | |
| Enable H pulse width (READ) | | tEWHR | | 140 | — | |
| Write data setup time | D[7:0] | tDS6 | | 40 | — | |
| Write data hold time | | tDH6 | | 10 | — | |
| Read data access time | | tACC6 | CL = 16 pF | — | 70 | |
| Read data output disable time | | tOH6 | CL = 16 pF | 5 | 50 | |

*1 The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr + tf) ≤ (tCYC6 – tEWLW – tEWHW) for (tr + tf) ≤ (tCYC6 – tEWLR – tEWHR) are specified.

*2 All timing is specified using 20% and 80% of VDD1 as the reference.

*3 tEWLW and tEWLR are specified as the overlap between CSB being "L" and E.

**System Bus Timing for 8080 Series MPU**




(VDD1 = 3.3V , Ta =25°C)

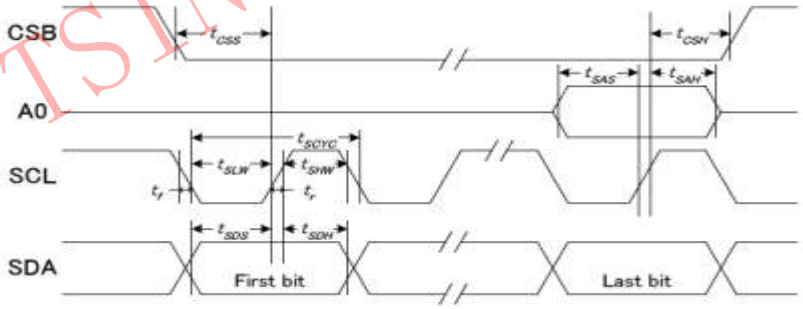
| Item | Signal | Symbol | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| Address setup time | A0 | tAW8 | | 0 | — | ns |
| Address hold time | | tAH8 | | 10 | — | |
| System cycle time | /WR | tCYC8 | | 240 | — | |
| /WR L pulse width (WRITE) | | tCCLW | | 80 | — | |
| /WR H pulse width (WRITE) | | tCCHW | | 80 | — | |
| /RD L pulse width (READ) | RD | tCCLR | | 140 | — | |
| /RD H pulse width (READ) | | tCCHR | | 80 | — | |
| WRITE Data setup time | D[7:0] | tDS8 | | 40 | — | |
| WRITE Data hold time | | tDH8 | | 20 | — | |
| READ access time | | tACC8 | CL = 16 pF | — | 70 | |
| READ Output disable time | | tOH8 | CL = 16 pF | 5 | 50 | |

*1 The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr + tf) ≦ (tCYC8 – tCCLW – tCCHW) for (tr + tf) ≦ (tCYC8 – tCCLR – tCCHR) are specified.

*2 All timing is specified using 20% and 80% of VDD1 as the reference.

*3 tCCLW and tCCLR are specified as the overlap between CSB being "L" and WR and RD being at the "L" level.

**System Bus Timing for 4-Line Serial Interface**




(VDD1 = 3.3V , Ta =25°C)

| Item | Signal | Symbol | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| Serial clock period | SCLK | tSCYC | | 50 | — | ns |
| SCLK "H" pulse width | | tSHW | | 25 | — | |
| SCLK "L" pulse width | | tSLW | | 25 | — | |
| Address setup time | A0 | tSAS | | 20 | — | |
| Address hold time | | tSAH | | 10 | — | |
| Data setup time | SDA | tSDS | | 20 | — | |
| Data hold time | | tSDH | | 10 | — | |
| CSB-SCLK time | CSB | tCSS | | 20 | — | |
| CSB-SCLK time | | tCSH | | 40 | — | |

*1 The input signal rise and fall time (tr, tf) are specified at 15 ns or less.

*2 All timing is specified using 20% and 80% of VDD1 as the standard.

# 5. COMMANDS AND FUNCTION DESCRIPTION

| INSTRUCTION | A0 | R/W (RWR) | COMMAND BYTE | | | | | | | | DESCRIPTION |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| (1) Display ON/OFF | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | D | D=1, display ON<br>D=0, display OFF |
| (2) Set Start Line | 0 | 0 | 0 | 1 | S5 | S4 | S3 | S2 | S1 | S0 | Set display start line |
| (3) Set Page Address | 0 | 0 | 1 | 0 | 1 | 1 | Y3 | Y2 | Y1 | Y0 | Set page address |
| (4) Set Column Address | 0 | 0 | 0 | 0 | 0 | 1 | X7 | X6 | X5 | X4 | Set column address (MSB) |
| | 0 | 0 | 0 | 0 | 0 | 0 | X3 | X2 | X1 | X0 | Set column address (LSB) |
| (5) Read Status | 0 | 1 | 0 | MX | D | RST | 0 | 0 | 0 | 0 | Read IC Status |
| (6) Write Data | 1 | 0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Write display data to RAM |
| (7) Read Data | 1 | 1 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Read display data from RAM |
| (8) SEG Direction | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | MX | Set scan direction of SEG<br>MX=1, reverse direction<br>MX=0, normal direction |
| (9) Inverse Display | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | INV | INV =1, inverse display<br>INV =0, normal display |
| (10) All Pixel ON | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | AP | AP=1, set all pixel ON<br>AP=0, normal display |
| (11) Bias Select | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | BS | Select bias setting<br>0=1/9; 1=1/7 (at 1/65 duty) |
| (12) Read-modify-Write | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | Column address increment:<br>Read:+0 , Write:+1 |
| (13) END | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | Exit Read-modify-Write mode |
| (14) RESET | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | Software reset |
| (15) COM Direction | 0 | 0 | 1 | 1 | 0 | 0 | MY | - | - | - | Set output direction of COM<br>MY=1, reverse direction<br>MY=0, normal direction |
| (16) Power Control | 0 | 0 | 0 | 0 | 1 | 0 | 1 | VB | VR | VF | Control built-in power circuit ON/OFF |
| (17) Regulation Ratio | 0 | 0 | 0 | 0 | 1 | 0 | 0 | RR2 | RR1 | RR0 | Select regulation resistor ratio |
| (18) Set EV | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Double command!! Set electronic volume (EV) level |
| | 0 | 0 | 0 | 0 | EV5 | EV4 | EV3 | EV2 | EV1 | EV0 | |
| (19) Set Booster | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | Double command!! Set booster level:<br>00=4X, 01=5X, 10=6X |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | BL1 | BL0 | |
| (20) Power Save | 0 | 0 | Compound Command | | | | | | | | Display OFF + All Pixel ON |
| (21) NOP | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | No operation |
| (22) Test | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | - | Do NOT use.<br>Reserved for testing. |

Note: Symbol "-" means this bit can be "H" or "L".

**Display ON/OFF**

The D flag selects the display mode.

| A0 | R/W(RWR) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | D |

D=1: Normal Display Mode.

D=0: Display OFF. All SEGs/COMs output with VSS.

**Set Start Line**

This instruction sets the line address of the Display Data RAM to determine the initial display line. The display data of the specified line address is displayed at the top row (COM0) of the LCD panel.

| A0 | R/W(RWR) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 1 | S5 | S4 | S3 | S2 | S1 | S0 |

| S5 | S4 | S3 | S2 | S1 | S0 | Line address |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 0 | 0 | 1 | 0 | 2 |
| 0 | 0 | 0 | 0 | 1 | 1 | 3 |
| : | : | : | : | : | : | : |
| 1 | 1 | 1 | 1 | 0 | 1 | 61 |
| 1 | 1 | 1 | 1 | 1 | 0 | 62 |
| 1 | 1 | 1 | 1 | 1 | 1 | 63 |

**Set Page Address**

Y [3:0] defines the Y address vector address of the display RAM.

| A0 | R/W(RWR) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 1 | 1 | Y3 | Y2 | Y1 | Y0 |

| Y3 | Y2 | Y1 | Y0 | Page Address | Valid Bit |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Page0 | D0~ D7 |
| 0 | 0 | 0 | 1 | Page1 | D0~ D7 |
| 0 | 0 | 1 | 0 | Page2 | D0~ D7 |
| : | : | : | : | : | : |
| 0 | 1 | 1 | 0 | Page6 | D0~ D7 |
| 0 | 1 | 1 | 1 | Page7 | D0~ D7 |
| 1 | 0 | 0 | 0 | Page8 (icon page) | D0 |

**Set Column Address of RAM**

The range of column address is 0...131. The parameter is separated into 2 instructions. The column address is increased (+1) after each byte of display data access (read/write). This allows MPU accessing DDRAM content continuously. This feature stops at the end of each page (Column Address "83h").

| A0 | R/W(RWR) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 1 | X7 | X6 | X5 | X4 |

| A0 | R/W(RWR) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | X3 | X2 | X1 | X0 |

| X7 | X6 | X5 | X4 | X3 | X2 | X1 | X0 | Column address |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 2 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 3 |
| : | : | : | : | : | : | : | : | : |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 129 |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 120 |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 131 |

**Read Status**

Read the internal status of ST7567. The read function is not available in serial interface mode.

| A0 | R/W(RWR) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | MX | D | RST | 0 | 0 | 0 | 0 |

| Flag | Description |
|---|---|
| MX | MX=0: Normal direction (SEG0->SEG131)<br>MX=1: Reverse direction (SEG131->SEG0) |
| D | D=0: Display ON<br>D=1: Display OFF |
| RST | RST=1: During reset (hardware or software reset)<br>RST=0: Normal operation |

**Write Data**

8-bit data of Display Data from the microprocessor can be written to the RAM location specified by the column address and page address. The column address is increased by 1 automatically so that the microprocessor can continuously write data to the addressed page. During auto-increment, the column address wraps to 0 after the last column is written.

| A0 | R/W(RWR) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 1 | 0 | Write Data | | | | | | | |

**Read Data**

8-bit data of Display Data from the RAM location specified by the column address and page address can be read to the microprocessor. The read function is not available in serial interface mode.

| A0 | R/W(RWR) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 1 | 1 | Read Data | | | | | | | |

**SEG Direction**

| A0 | R/W(RWR) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | MX |

| Flag | Description |
|---|---|
| MX | MX=0: Normal direction (SEG0->SEG131)<br>MX=1: Reverse direction (SEG131->SEG0) |

**Inverse Display**

This instruction changes the selected and non-selected voltage of SEG. The display will be inversed (white -> Black, Black -> White) while the display data in the Display Data RAM is never changed.

| A0 | R/W(RWR) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | INV |

| Flag | Description |
|---|---|
| INV | INV=0: Normal display<br>INV =1: Inverse display |

**All Pixel ON**

This instruction will let all segments output the selected voltage and make all pixels turned ON.

| A0 | R/W(RWR) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | AP |

| Flag | Description |
|---|---|
| AP | AP =0: Normal display<br>AP =1: All pixels ON |

**Bias Select**

Select LCD bias ratio of the voltage required for driving the LCD.

| A0 | R/W(RWR) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | BS |

| Duty | Bias | |
|---|---|---|
| | BS=0 | BS=1 |
| 1/65 | 1/9 | 1/7 |
| 1/49 | 1/8 | 1/6 |
| 1/33 | 1/6 | 1/5 |
| 1/55 | 1/8 | 1/6 |

Reference LCD Bias Voltage (1/65 Duty with 1/9 Bias)

| Symbol | Bias Voltage |
|---|---|
| V0 | V0 |
| VG | 2/9 x V0 |
| VM | 1/9 x V0 |
| VSS | VSS |

Please Note:

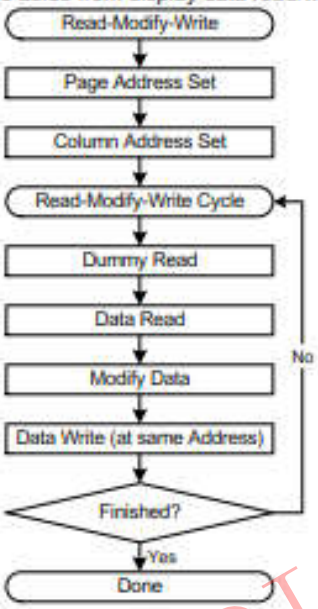
* VG range: 1.24V ≤ VG < VDD2.
* VM range: 0.62V ≤ VM < VDD2.

**Read-modify-Write**

This command is used paired with the "END" instruction. Once this command has been input, the display data read operation will not change the column address, but only the display data write operation will increase the column address (X[7:0]+1). This mode is maintained until the END command is input. This function makes it possible to reduce the load on the MPU when there are repeating data changes in a specified display region, such as a blanking cursor.

| A0 | R/W(RWR) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

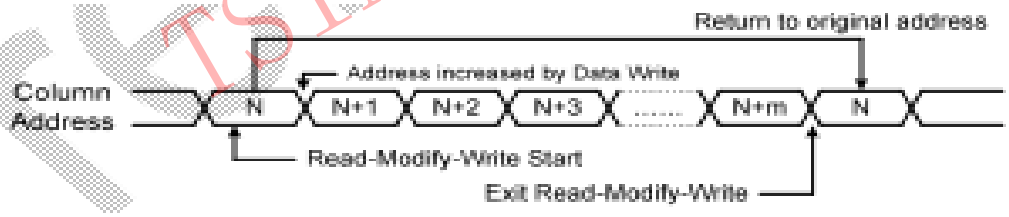
* In Read-modify-Write mode, other instructions aside from display data read/write commands can also be used.




**END**

When the END command is input, the Read-modify-Write mode is released and the column address returns to the address it was when the Read-modify-Write instruction was entered.

| A0 | R/W(RWR) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 |




**RESET**

This instruction resets Start Line (S[5:0]), Column Address (X[7:0]), Page Address (Y[3:0]) and COM Direction (MY) to their default setting. Please note this instruction is not complete same as hardware reset (RSTB=L) and cannot initialize the built-in power circuit which is initialized by the RSTB pin. The detailed information is in "Section 7. RESET CIRCUIT".

| A0 | R/W(RWR) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 |

### COM Direction

This instruction controls the common output status which changes the vertical display direction. The detailed information can be found in Fig 9.

| A0 | R/W(RWR) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 1 | 0 | 0 | MY | - | - | - |

| Flag | Description |
|---|---|
| MY | MY=0: Normal direction (COM0->COM63)<br>MY=1: Reverse direction (COM63->COM0) |

### Power Control

This instruction controls the built-in power circuits. Typically, these 3 flags are turned ON at the same time.

| A0 | R/W(RWR) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | VB | VR | VF |

| Flag | Description |
|---|---|
| VB | VB=0: Built-in Booster OFF<br>VB=1: Built-in Booster ON |
| VR | VR=0: Built-in Regulator OFF<br>VR=1: Built-in Regulator ON |
| VF | VF=0: Built-in Follower OFF<br>VF=1: Built-in Follower ON |

### Regulation Ratio

This instruction controls the regulation ratio of the built-in regulator.

| A0 | R/W(RWR) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | RR2 | RR1 | RR0 |

| RR2 | RR1 | RR0 | Regulation Ratio (RR) |
|---|---|---|---|
| 0 | 0 | 0 | 3.0 |
| 0 | 0 | 1 | 3.5 |
| 0 | 1 | 0 | 4.0 |
| 0 | 1 | 1 | 4.5 |
| 1 | 0 | 0 | 5.0 |
| 1 | 0 | 1 | 5.5 |
| 1 | 1 | 0 | 6.0 |
| 1 | 1 | 1 | 6.5 |

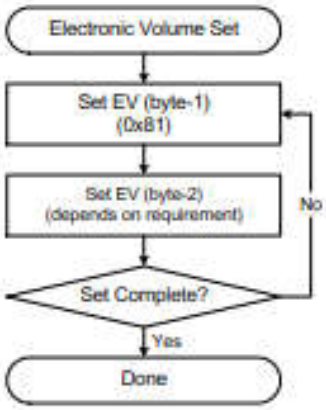
The operation voltage (V0) calculation formula is shown below: (RR comes from Regulation Ratio, EV comes from EV[5:0])
V0 = RR X [ 1 – (63 – EV) / 162 ] X 2.1, or **V0 = RR X [ ( 99 + EV ) / 162 ] X 2.1**

| SYMBOL | REGISTER | VALUE |
|---|---|---|
| RR | RR[2:0] | 3, 3.5, 4, 4.5, 5, 5.5, 6 and 6.5 |
| EV | EV[5:0] | 0~63 |

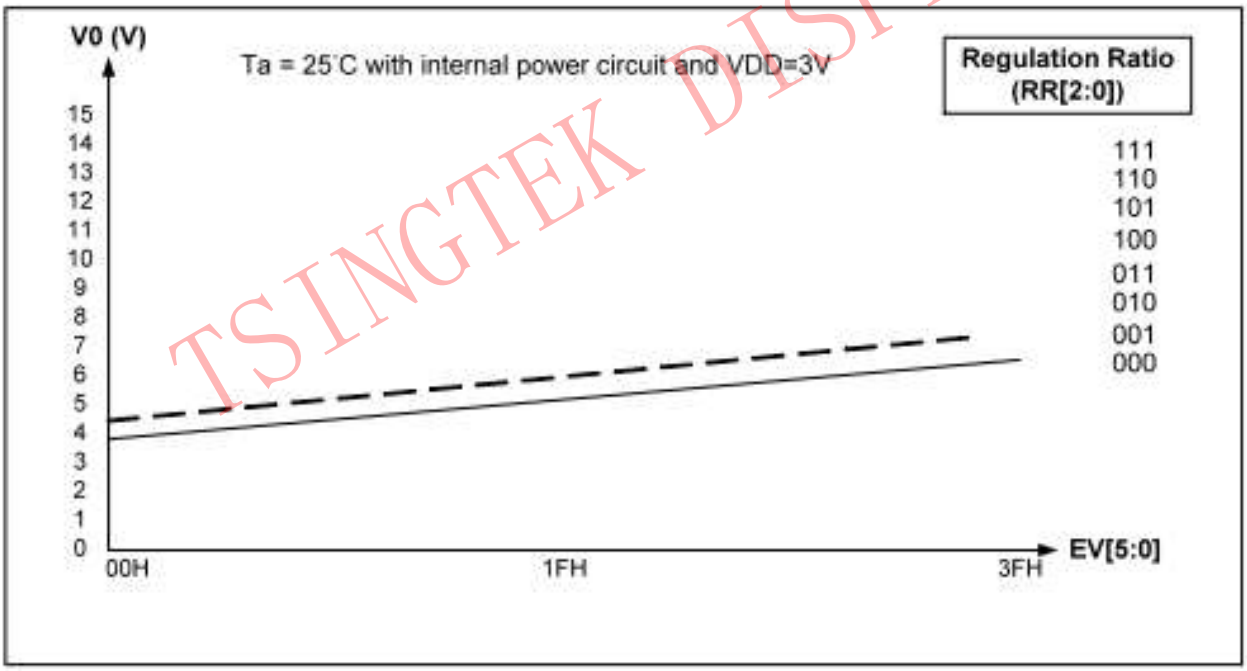
**Set EV**

This is double byte instruction. The first byte set ST7567 into EV adjust mode and the following instruction will change the EV setting. That means these 2 bytes must be used together. They control the electronic volume to adjust a suitable V0 voltage for the LCD.

| A0 | R/W(RWR) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 | EV5 | EV4 | EV3 | EV2 | EV1 | EV0 |




The maximum voltage that can be generated is dependent on the VDD2 voltage and the loading of LCD module. There are 8 V0 voltage curve can be selected. It is recommended the EV should be close to the center (1FH) for easy contrast adjustment. Please refer to the "Selection of Application Voltage" section for detailed information.



### Power Save (Compound Instruction)

This is compound instruction. The 1st instruction is Display OFF (D=0) and the 2nd instruction is All Pixel ON (AP=1). The Power Save mode starts the following procedure: (the display data and register settings are still kept except D-Flag and AP-Flag)

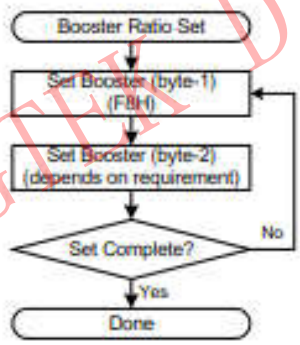
1. Stops internal oscillation circuit;
2. Stops the built-in power circuits;
3. Stops the LCD driving circuits and keeps the common and segment outputs at VSS.


After exiting Power Save mode, the settings will return to be as they were before.

### Set Booster

This is double byte instruction. The first byte set ST7567 into booster configuration mode and the following instruction will change the booster setting. That means these 2 bytes must be used together. They control the built-in booster circuit to provide the power source of the built-in regulator. ST7567 booster is built-in booster capacitors. The only external component is a keep capacitor between V0 and XV0. Booster level can be changed with instruction only without changing hardware connection.

| A0 | R/W(RWR) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | BL1 | BL0 |






### NOP

"No Operation" instruction. ST7567 will do nothing when receiving this instruction.

| A0 | R/W(RWR) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |

### Test

The test mode is reserved for IC testing. Please don't use this instruction. If the test mode is enabled accidentally, it can be cleared by: issuing an "L" pulse on RSTB pin, issuing RESET instruction or issuing NOP instruction.

| A0 | R/W(RWR) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | - |

Note: "-" means "1" or "0".

# 6. QUALITY SPECIFICATIONS

## 6.1 ACCEPTABLE QUALITY LEVEL

| Inspection items | Sampling procedures | AQL |
|---|---|---|
| Electro-optical tests | GB/T2828.1-2012<br>Inspection level Ⅱ<br>Normal inspection<br>Single sample inspection | 0.65 |
| Non Electro-optical tests<br>and<br>Dimension measurement | GB/T2828.1-2012<br>Inspection level Ⅱ<br>Normal inspection<br>Single sample inspection | 1.5 |

## 6.2 ENVIRONMENT

-Room temperature: 23±5 ºC
-Humidity: 55±15%RH

# 7. RELIABILITY

| Test Item | Content of Test | Test Condition |
|---|---|---|
| High temperature storage | Endurance test of high storage temperature for a long time | 80°C, 96hrs |
| Low temperature storage | Endurance test of low storage temperature for a long time | -40°C, 96hrs |
| High temperature operation | Endurance test of operating at high temperature for a long time | 80°C,96hrs |
| Low temperature operation | Endurance test of operating at low temperature for a long time | -30°C,96hrs |
| High temperature /Humidity storage | Endurance test applying the high temperature and high humidity storage for a long time | 60°C,90%RH<br>96hrs |
| Temperature cycle | Endurance test applying the low and high temperatures<br>Temperature cycle:<br>-30°C→25°C→80°C<br>30min←5min←30min<br>1 cycle | -30°C/80°C<br>10 cycle |
| Vibration test | Endurance test applying the vibration | 10~55Hz,1.5mmp-p<br>One cycle 60 seconds<br>to 3 directions of<br>X,Y,Z |

Note 1: Condensation of water is not permitted on the module.

Note 2: The module should be inspected after 4 hour storage in normal conditions .

# 8. PRECAUTIONS

（1）Avoid any intense shock, impact, extrusion and falls from a height.

（2）Neither disassemble nor modify the display module.

（3）The polarizer covering display surface is soft and easily scratched, please be careful when handling the display module.

（4）When cleaning the display surface please use a soft cloth with recommended solvent (listed below) and wipe gently: - Isopropyl alcohol -Ethyl alcohol.
Do not wipe the display surface with dry or hard materials as this will damage the polarized surface. Do not use the following solvents:
-Water -Ketone - Aromatics

（5）Pay sufficient attention to the working environments when handing display modules .

- Be sure to make human body ground.
- Be sure to ground tools such as soldering irons while using them.
- Avoid working under dry environments to prevent generating static electricity.
- Be careful of static electricity while peeling off protective films on display module surfaces.

（6）Soldering should be performed only on the I/O terminals.

（7）Do not apply input signals while the logic power is off.

（8）The absolute maximum ratings of display module cannot be exceeded, and if exceeded, damages may happen.

（9）Under the maximum operating temperature, 50%RH or less is required.

（10）Storage: please storage in anti-static electricity container and clean environment. The reasonable storage method is low humidity, temperature from 0℃ to 35℃.

（11）Please feel free to contact TSINGTEK DISPLAY if you have any other questions.