Atmel AVR127: Understanding ADC parameters

Features

- **Getting introduced to ADC concepts**
- **Understanding various ADC parameters**
- **Understanding the effect of ADC parameters on the accuracy of the ADC**

1 Introduction

This application note discusses about the basic concepts of analog-to-digital converter (ADC) and the various parameters that determine the performance of an ADC. These ADC parameters are of good importance since they are a part of deciding the accuracy of the ADC's output.

The parameters of an ADC can be broadly classified into static performance parameters and dynamic performance parameters. Static performance parameters are those parameters that are not related to ADC's input signal. These parameters are measured and analyzed for all types of ADCs (ADCs integrated within the microcontroller to standalone ADCs whose operating frequency are usually higher). Conversely, dynamic performance parameters are related to ADC's input signal and their effects are significant with higher frequencies.

Major static parameters include gain error, offset error, full scale error and linearity errors whereas some important dynamic parameters include signal-to-noise ratio (SNR), total harmonic distortion (THD), signal to noise and distortion (SINAD) and effective number of bits (ENOB).

This application note is for guidance and we recommend the designer to refer to specific Atmel® device datasheet for more details.

8-bit Atmel Microcontrollers

Application Note

Rev. 8456A-AVR-11/11

2 Basic concepts

An ADC is a simple electronic system or a module that has analog input, reference voltage input and digital outputs. The ADC translates the analog input signal to a digital output value that represents the size of the analog input relative to the reference voltage. It basically samples the input analog voltage and produces an output digital code for each sample taken.

Figure 2-1. Basic diagram of ADC.

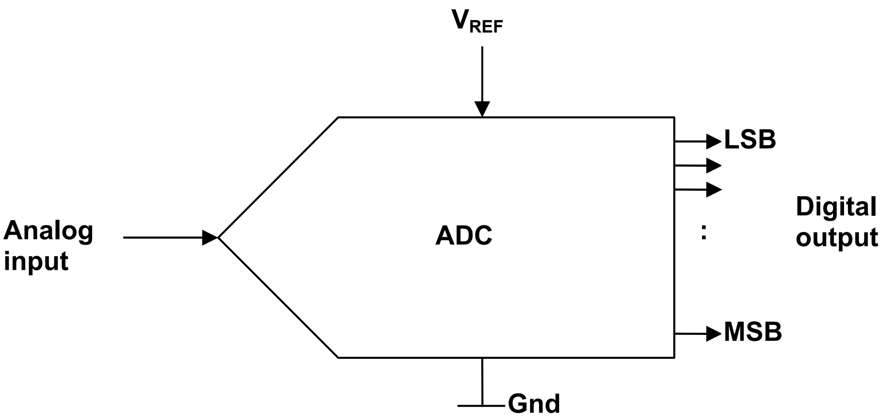


Figure 2-1 shows the basic symbol of an ADC with the input and output signals used.

To get a better picture about the ADC concepts, let us first look into some basic ADC terms used.

2.1 Input voltage range

The input voltage range of an ADC is determined by the reference voltage (V_{REF}) applied to the ADC. A reference voltage is the voltage that is applied either internally or externally by applying voltage on an external pin of the microcontroller; the selection of reference voltage can be made from the reference configuration bits available in the microcontroller. ADC's do not covert the input analog voltage to a valid digital output which is more then the reference voltage, it is the responsibility of designer to make sure that the analog input voltage does not exceed the reference voltage. This means operating the ADC with an input analog voltage greater than the reference voltage will saturate the ADC and ADC outputs the highest digital code value. The input voltage range is also called as conversion range.

Some type of ADC's when operated in signed mode (the mode which produces signed output codes) will allow negative analog input voltages. In such cases the analog input range is from $-V_{REF}$ to $+V_{REF}$. This negative reference setting will be taken care by the internal analog circuits in many cases.

An ADC which accepts both positive and negative input voltages is called as bipolar ADC whereas an ADC that accepts only positive input voltage is called as unipolar ADC.

2.2 Resolution

The entire input voltage range (from 0V to V_{REF}) is divided into number of sub ranges in such a way that each sub range is assigned a single output digital code. A sub range is also called LSB (least significant bits) and the number of sub ranges is usually in powers of two. The total number of sub ranges is called the resolution of the ADC. For an example, an ADC having eight LSBs has the resolution of eight or three bits ($2^3 = 8$). If an ADC's resolution is three bits then it also means that the code width of the output is three bits.

2.3 Quantization

The LSBs are formed so that a range of input voltages is assigned to a single output digital code. For example, consider an ADC with V_{REF} as 2V and resolution as three bits. Now the 2V is divided into eight LSBs so that each LSB is in the range of 250mV. Now an input voltage of 0V as well as input voltage of 250mV is assigned to the same output digital code 000. This process is called as quantization.

2.4 Conversion mode

A conversion mode is a method in which the ADC processes the input and performs the conversion operation. A standard ADC has basically two types of conversion modes.

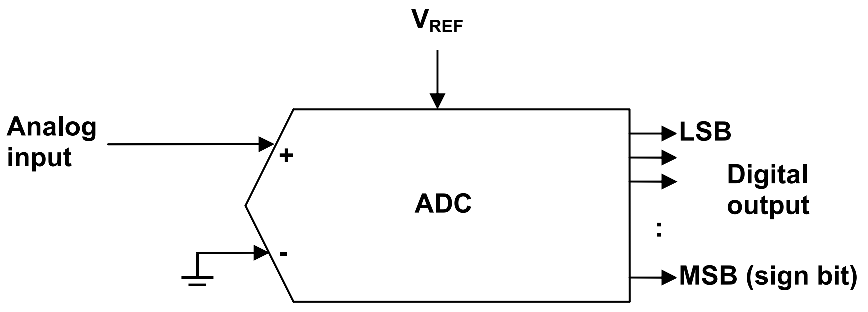
1. Single ended conversion mode.
2. Differential conversion mode.

2.4.1 Single ended conversion

In single ended conversion, only one analog input is taken and the ADC sampling and conversion is done for that input. In single ended conversion ADC can be configured to operate in unsigned or signed mode for which ADC's will have inverting and non-inverting inputs that are internal.

For example in signed mode of operation, the single-ended input may be given to the non-inverting input of the ADC and the inverting input of the ADC is grounded. This is depicted in Figure 2-2. In this case the reference voltage is from – V_{REF} to + V_{REF}, which means it allows negative input voltages.

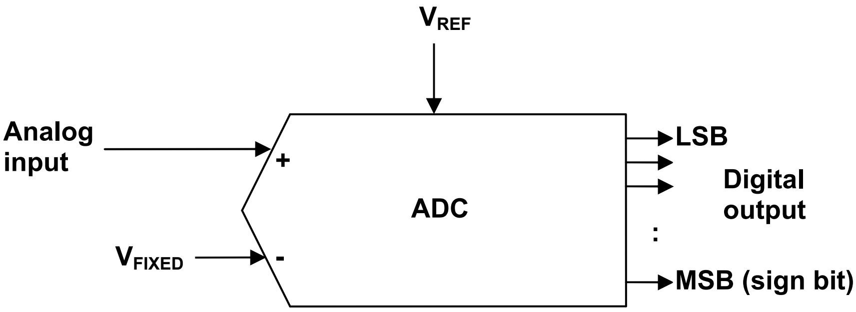
Figure 2-2. ADC in signed single-ended mode.



In unsigned single-ended mode, the single-ended input is given to the non-inverting input of the ADC as before and the inverting input of the ADC is supplied with some fixed voltage value (V_{FIXED} which is usually half of the reference voltage minus a fixed

offset) as shown in Figure 2-3. In this case the input voltage range is from 0V to V_{REF}, which means it does not allows negative input voltages.

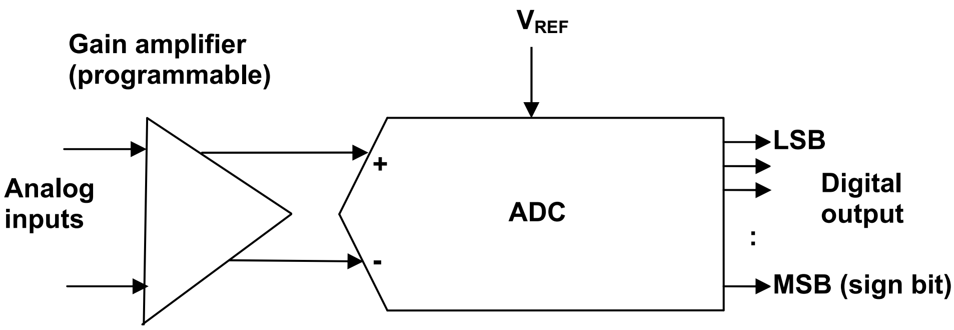
Figure 2-3. ADC in unsigned single-ended mode.



2.4.2 Differential conversion

In differential conversion mode, two analog inputs are taken and applied to the inverting and non-inverting inputs of the ADC, either directly or after doing some amplification by selecting some programmable amplification stages (gain amplifier stage). Differential conversions are usually operated in signed mode, where the MSB of the output code acts as the sign bit. Also the reference voltage is from - V_{REF} to $+V_{REF}$ for signed mode. This is shown in the Figure 2-4.

Figure 2-4. ADC in differential mode.



2.5 Ideal ADC

An ideal ADC is just a theoretical concept, and cannot be implemented in real life. It has infinite resolution, where every possible analog input value gives a unique digital output from the ADC within the specified conversion range. An ideal ADC can be described mathematically by a straight-line transfer function, as shown in Figure 2-5 and Figure 2-6.

Figure 2-5. Single ended ADC.

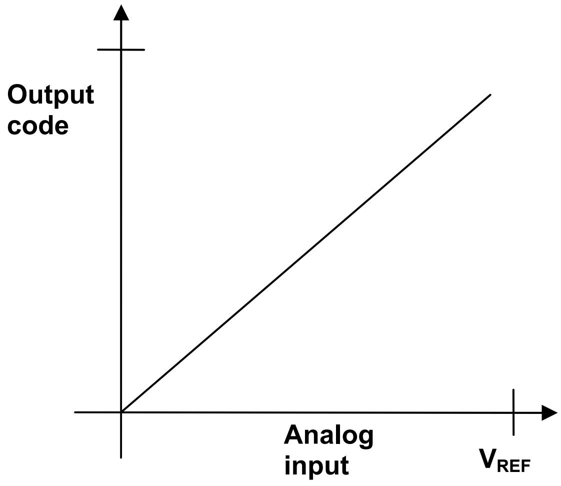
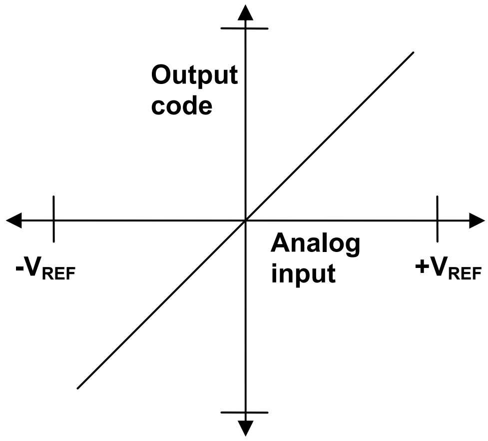


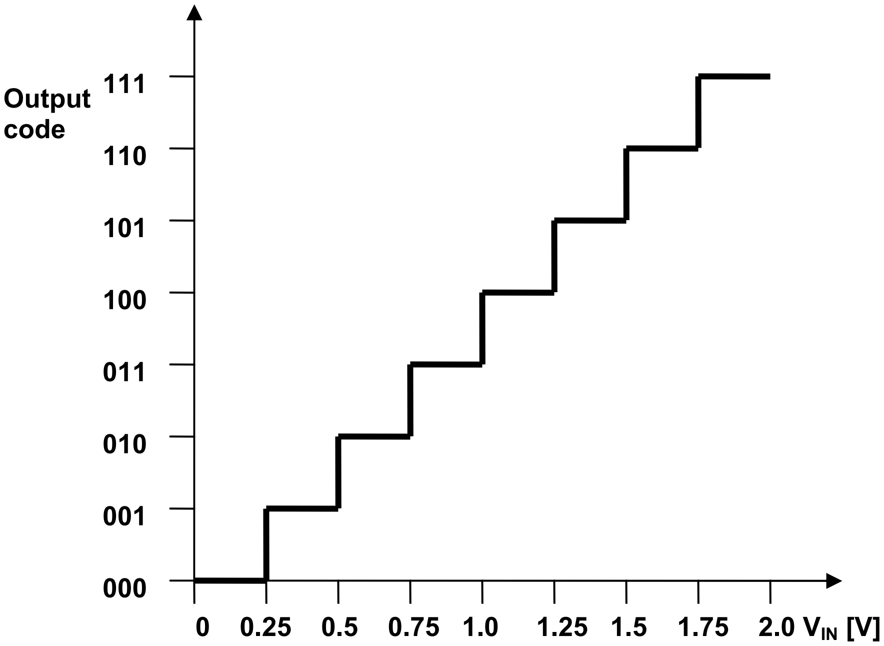
Figure 2-6. Differential ADC.



2.6 Perfect ADC

To define a perfect ADC, the concept of quantization must be used. Due to the digital nature of an ADC, continuous output values are not possible. The perfect ADC performs the quantization process during conversion. This results in a staircase transfer function where each step represents one LSB.

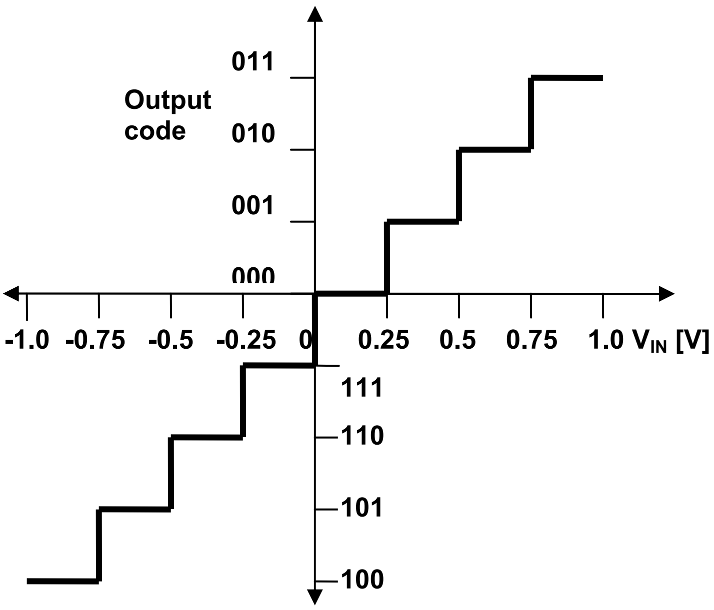
Figure 2-7. Transfer function of 3-bit ADC (unadjusted quantization) (single ended).



If the reference voltage is 2V, say, and the ADC resolution is three bits, then the step width becomes 250mV (1LSB). The input analog voltage range from 0V to 250mV will be assigned the digital output code 000 and the input analog voltage range from 250mV to 500mV will be assigned the digital code 001 and so on. This is depicted in Figure 2-7 which shows the transfer function of a perfect 3-bit ADC operating in single ended mode. Figure 2-8, given below, shows the transfer function of a perfect 3-bit ADC operating in differential mode.

NOTE The reference voltage is from -1V to +1V in this case and the MSB acts as sign bit.

Figure 2-8. Transfer function of 3-bit ADC (unadjusted quantization) (differential).



From the Figure 2-7, it is obvious that an input voltage of 0V produces an output code 000. At the same time, an input voltage of 250mV also produces the same output code 000 which is an error due to the process of quantization. This error is called as quantization error. As the input voltage rises from 0V, the quantization error also rises from 0LSB and reaches a maximum quantization error of 1LSB at 250mV. Again the quantization error increases from 0LSB to 1LSB as the input rises from 250mV to 500mV.

This maximum quantization error of 1LSB can be reduced to ±0.5LSB by shifting the transfer function towards left through 0.5LSB.

Figure 2-9. Transfer function of 3-bit ADC (adjusted quantization) (single ended).

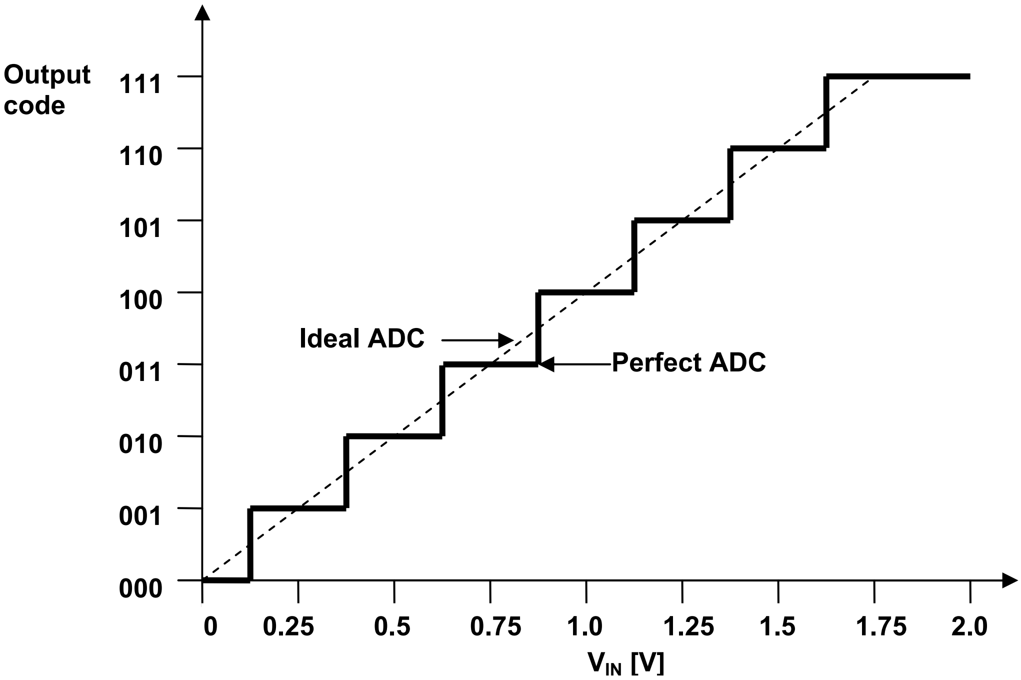
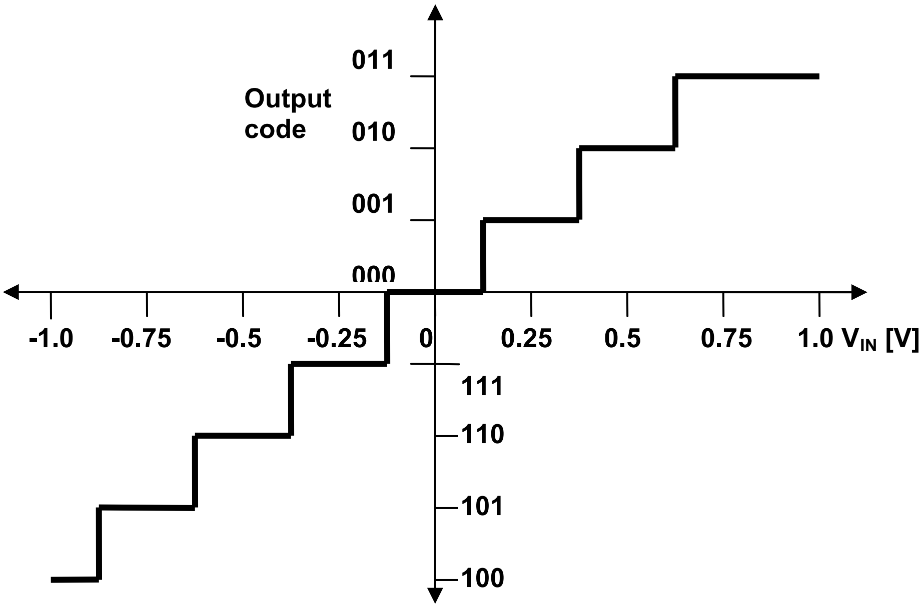


Figure 2-9 depicts the quantization adjusted perfect transfer function together with the ideal transfer function. As seen on the figure, the perfect ADC equals the ideal ADC on the exact midpoint of every step. This means that the perfect ADC essentially rounds input values to the nearest output step value. Similarly Figure 2-10 is for differential ADC.

Figure 2-10. Transfer function of 3-bit ADC (adjusted quantization) (differential).



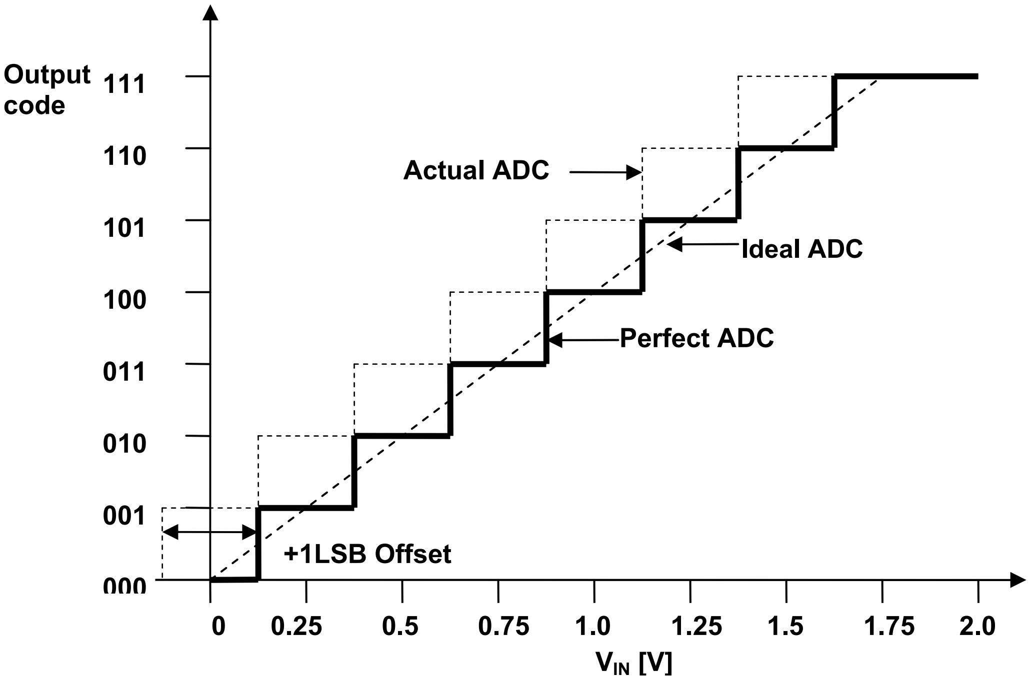
Quantization error is the only error when perfect ADC is considered. But in case of real ADC, there are several other errors other than quantization error as explained below.

2.7 Offset error

The offset error is defined as the deviation of the actual ADC's transfer function from the perfect ADC's transfer function at the point of zero to one transition measured in LSB.

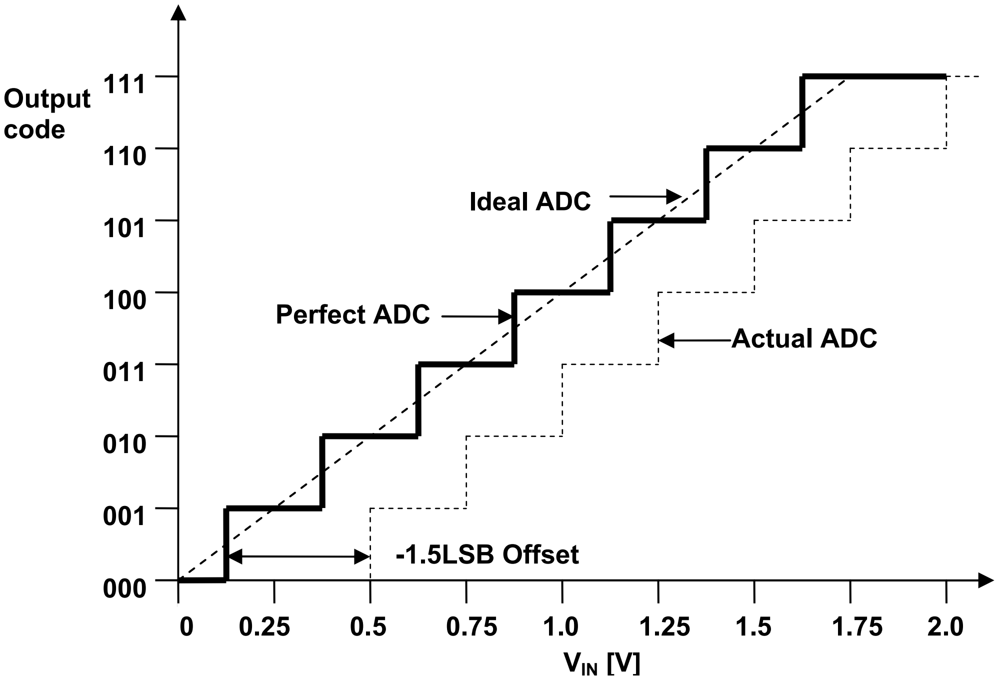
When the transition from output value 0 to 1 does not occur at an input value of 0.5LSB, then we say that there is an offset error. With positive offset errors, the output value is larger than 0 when the input voltage is less than 0.5LSB from below. With negative offset errors, the input value is larger than 0.5LSB when the first output value transition occurs. In other words, if the actual transfer function lies below the ideal line, there is a negative offset and vice versa. Positive and negative offsets are shown in Figure 2-11 and Figure 2-12 respectively measured with double ended arrows.

Figure 2-11. Positive offset error.



In Figure 2-11, the first transition occurs at 0.5LSB and the transition is from 1 to 2. But 1 to 2 transitions should occur at 1.5LSB for perfect case. So the difference (Perfect – Real = 1.5LSB – 0.5LSB = +1LSB) is the offset error. Similarly in the Figure 2-12, the first transition occurs at 2LSB and the transition is from 0 to 1. But 0 to 1 transition should occur at 0.5LSB for perfect case. So the difference (Perfect – Real = 0.5LSB – 2LSB = -1.5LSB) is the offset error.

Figure 2-12. Negative offset error.



It should be noted that offset errors limit the available range for the ADC. A large positive offset error causes the output value to saturate at maximum before the input voltage reaches maximum. A large negative offset error gives output value 0 for the smallest input voltages.

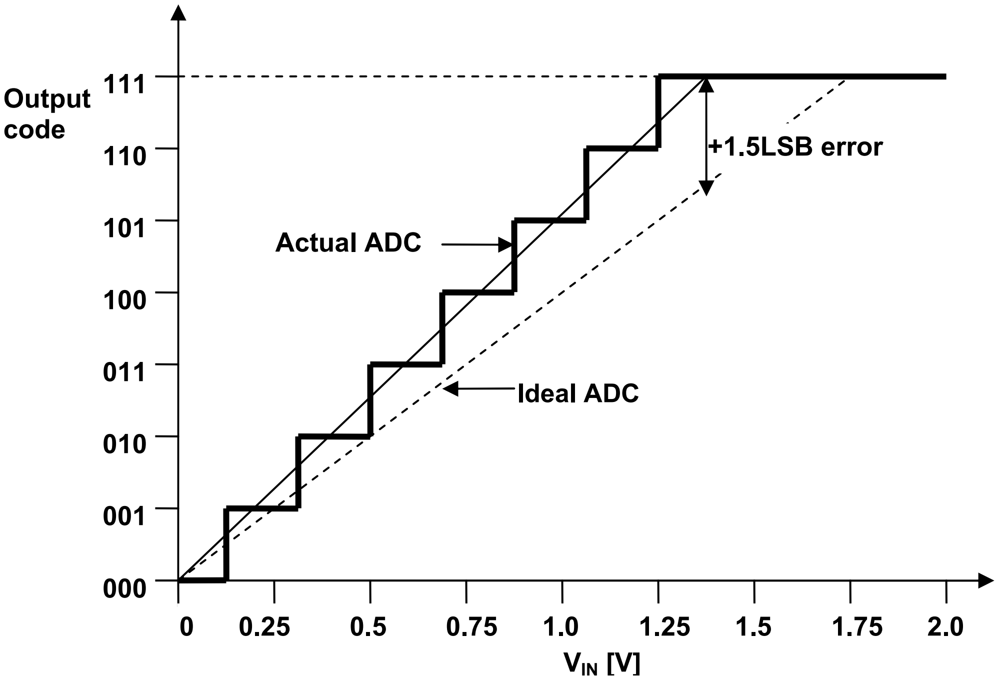
2.8 Gain error

The gain error is defined as the deviation of the last step's midpoint of the actual ADC from the last step's midpoint of the ideal ADC, after compensating for offset error.

After compensating for offset errors, applying an input voltage of 0 always give an output value of 0. However, gain errors cause the actual transfer function slope to deviate from the ideal slope. This gain error can be measured and compensated for by scaling the output values.

The example of a 3-bit ADC transfer function with gain errors is shown in Figure 2-13 and Figure 2-14.

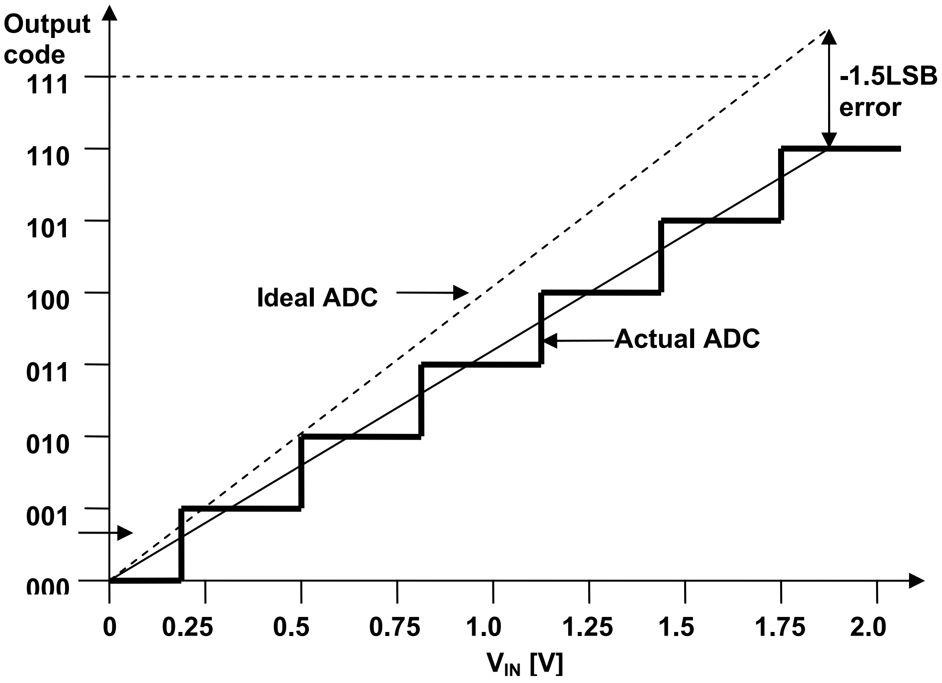
Figure 2-13. Positive gain error.



If the transfer function of the actual ADC occurs above the ideal straight line, then it produces positive gain error and vice versa. The gain error is calculated as LSBs from a vertical straight line drawn between the midpoint of the last step of the actual transfer curve and the ideal straight line.

In Figure 2-13, the output value saturates before the input voltage reaches its maximum. The vertical arrow shows the midpoint of the last output step. In Figure 2-14, the output value has only reached six when the input voltage is at its maximum. This results in a negative deviation for the actual transfer function.

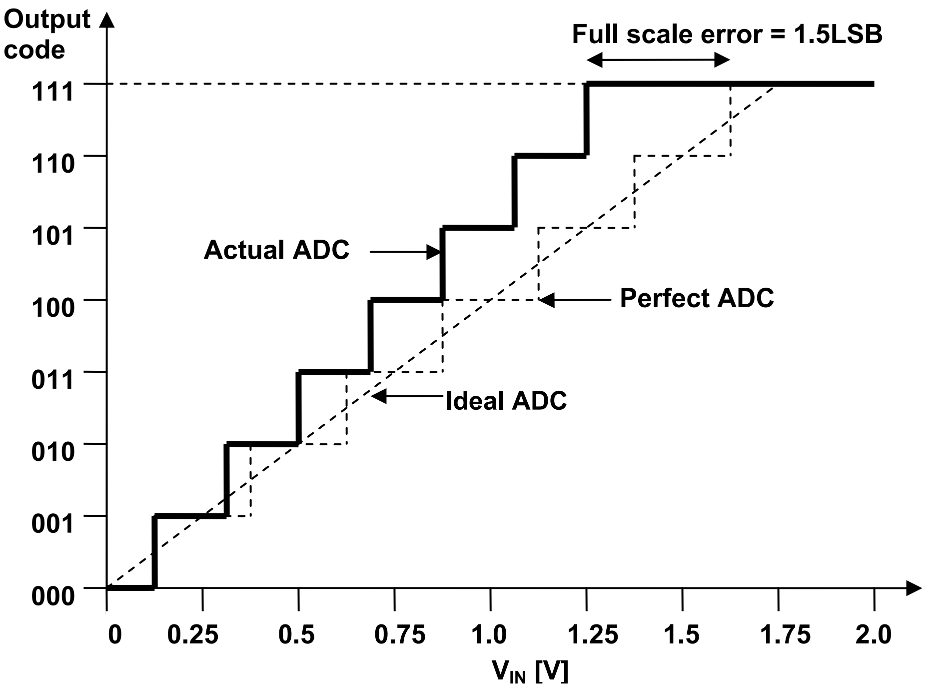
Figure 2-14. Negative gain error.



2.9 Full scale error

Full scale error is the deviation of the last transition (full scale transition) of the actual ADC from the last transition of the perfect ADC, measured in LSB or volts. Full scale error is due to both gain and offset errors.

Figure 2-15. Full scale error.



In Figure 2-15, the deviation of the last transitions between the actual and ideal ADC is 1.5LSB.

2.10 Non-linearity

The gain and offset errors occurring in the ADC can be measured and compensated using some calibration procedures. When offset and gain errors are compensated for, the actual transfer function should now be equal to the transfer function of perfect ADC. However, non-linearity in the ADC may cause the actual curve to deviate slightly from the perfect curve, even if the two curves are equal around 0 and at the point where the gain error was measured.

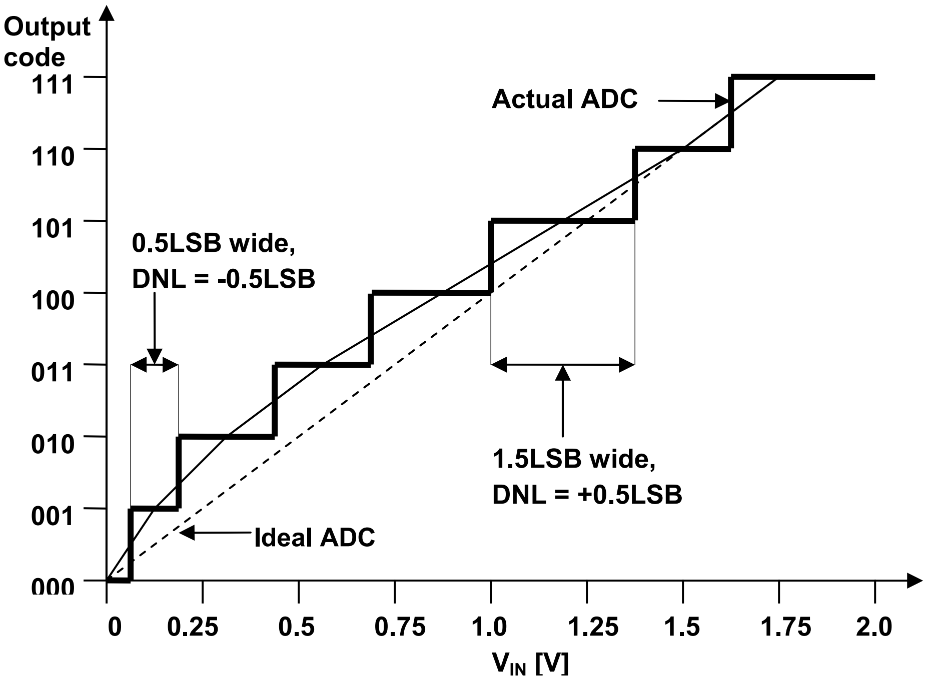
There are two major types of non-linearity's that degrade the performance of an ADC. They are differential non-linearity (DNL) and integral non-linearity (INL).

2.10.1 Differential non-linearity (DNL)

Differential non-linearity (DNL) is defined as the maximum and minimum difference between the step width and the perfect width (1LSB) of any output step.

Non-linearity produces quantization steps with varying widths. All steps should be one LSB wide, but some are narrower or wider.

Figure 2-16. Plot showing differential non-linearity (DNL).



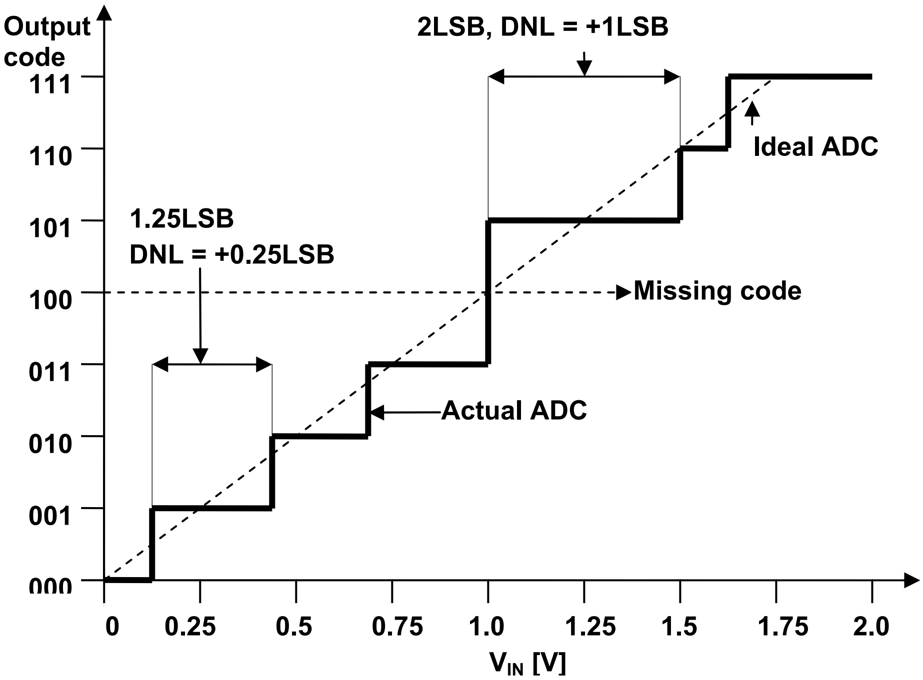
For the case of ideal ADC, the step width should be 1LSB. But an ADC with DNL shows step widths which are not exactly 1LSB. In Figure 2-16, in a maximum case the width of the step with output value 101 is 1.5LSB which should be 1LSB. So the DNL in this case would be +0.5LSB. Whereas in a minimum case, the width of the step with output value 001 is only 0.5LSB which is 0.5LSB less than the expected width. So the DNL now would be -0.5LSB.

2.10.2 Missing code

There are some special cases wherein the actual transfer function of the ADC would look as in the Figure 2-17.

In the example below, the first code transition (from 000 to 001) is caused by an input change of 250mV. This is exactly as it should be. The second transition, from 001 to 010, has an input change that is 1.25LSB, so is too large by 0.25LSB. The input change for the third transition is exactly the right size. The digital output remains constant when the input voltage changes from 1000mV to 1500mV and the code 100 can never appear at the output. It is missing. The severity of the missing code is less when the resolution of the ADC is higher. An ADC with DNL error less than ±1LSB guarantees no missing code.

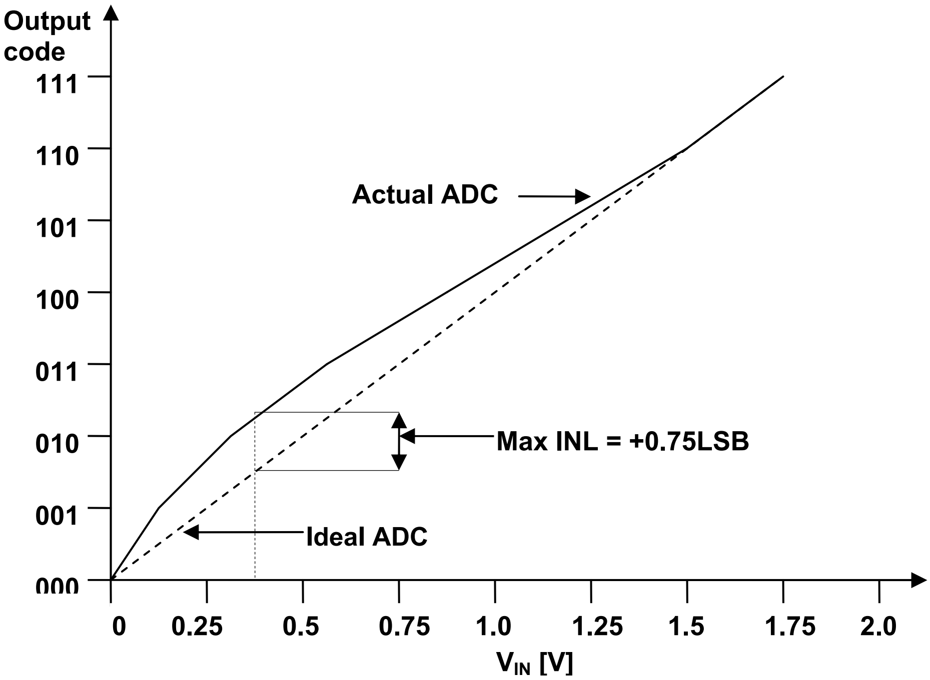
Figure 2-17. 3-bit ADC showing missing code.



2.10.3 Integral non-linearity (INL)

Integral non-linearity (INL) is defined as the maximum vertical difference between the actual and the ideal curve. It indicates the amount of deviation of the actual curve from the ideal transfer curve.

Figure 2-18. Plot showing integral non-linearity (INL).



INL can be interpreted as a sum of DNLs. For example several consecutive negative DNLs raise the actual curve above the ideal curve as shown in Figure 2-16 and the INL in this case would be positive. Negative INLs indicate that the actual curve is below the ideal curve. This means that the distribution of the DNLs determines the integral linearity of the ADC.

The INL can be measured by connecting the midpoints of all output steps of actual ADC and finding the maximum deviation from the ideal curve in terms of LSBs. From the Figure 2-18, we can note that the maximum INL is +0.75LSB.

2.11 Absolute error

Absolute error or absolute accuracy is the total uncompensated error and includes quantization error, offset error, gain error and non-linearity. So in a perfect case, the absolute error is 0.5LSB which is due to the quantization error. Gain and offset errors are more significant contributors of absolute error.

The absolute error represents a reduction in the ADC range, and one should therefore consider the margins to the minimum and maximum input values to avoid clipping keeping the absolute error in mind.

2.12 Signal to noise ratio (SNR)

SNR is defined as the ratio of the output signal voltage level to the output noise level. It is usually represented in decibels (dBs) and calculated with the following formula.

$$SNR(dB) = 20\log\left(\frac{V_{RMS(Signal)}}{V_{RMS(Noise)}}\right)$$

For example if the output signal amplitude is 1V(RMS) and the output noise amplitude is 1mV(RMS), then the SNR value would be 60dB. For good performance, the SNR value should be high. The above mentioned formula is a general definition for SNR.

The SNR value of an ideal ADC is given by:

SNR (dB) = 6.02N+1.76(dB)

where N is the resolution (no. of bits) of the ADC. For example an ideal 10-bit ADC will have an SNR of approximately 62dB.

2.13 Total harmonic distortion (THD)

Whenever an input signal of a particular frequency passes through a non-linear device, additional content is added at the harmonics of the original frequency. For example, assume an input signal having frequency f. Then the harmonic frequencies are 2f, 3f, 4f, etc. So non-linearity in the converter will produce harmonics that were not present in the original signal. These harmonic frequencies usually distort the output which degrades the performance of the system. This effect can be measured using the term called total harmonic distortion (THD).

THD is defined as the ratio of the sum of powers of the harmonic frequency components to the power of the fundamental/original frequency component. In terms of RMS voltage, the THD is given by,

$$THD = \frac{\sqrt{V_2^2 + V_3^2 + \ldots + V_n^2}}{V_1}$$

The THD should have minimum value for less distortion. As the input signal amplitude increases, the distortion also increases. The THD value also increases with the increase in the frequency.

2.14 Signal to noise and distortion (SINAD)

Signal to noise and distortion (SINAD) is a combination of SNR and THD parameters. It is defined as the ratio of the RMS value of the signal amplitude to the RMS value of all other spectral components, including harmonics, but excluding DC. For representing the overall dynamic performance of an ADC, SINAD is a good choice since it includes both the noise and distortion components.

SINAD can be calculated with SNR and THD as given below.

$$SINAD = -10\log\left(10^{-SNR/10} + 10^{-THD/10}\right)$$

2.15 ENOB

Effective number of bits (ENOB) is the number of bits with which the ADC when operated behaves like a perfect ADC. It is another way of representing the signal to noise ratio and distortion (SINAD) and is derived from the formula specified in Section 2.11 as given below:

$$ENOB = \frac{SINAD - 1.76}{6.02}$$

2.16 ADC timings

Basically an ADC takes some time for startup, sampling and holding and for conversion. Out of these, the startup time is more concerned with ADCs of high end microcontrollers that operate at higher frequencies.

2.16.1 Startup time

Startup time contains the minimum time (in clock cycles) needed to guarantee the best converted value after the ADC has been enabled either for the first time or after a wake up from some of the sleep modes.

2.16.2 Sample and hold time

Usually after giving a trigger to an ADC to start a conversion, it take some time (in clock cycles) to charge the internal capacitor to a stable value so that the conversion result is accurate. This time is called as sample time. This time also comes into picture when multiple channels are used during conversion. In this case it is the minimum time (in clock cycles) needed to guarantee the best converted value between two ADC channel selections. After the sampling time, the number of clock cycles it takes for the internal conversion circuitry to convert the charge or the voltage across the internal sampling capacitor into corresponding digital code is called as the hold time.

2.16.3 Settling time

When using multiple channels, there may be cases in which each channel may have different gain and offset configurations. Switching between these channels requires some amount of time, before beginning the sample and hold phase, in order to have good results. Especially care should be taken when switching between differential channels. Once a differential channel is selected, the ADC should wait for some amount of time for some of the analog circuits (for example the automatic offset cancellation circuitry) to stabilize to the new value. This time is called as settling time. So ADC conversion should not be started before this time. Doing so will produce an erroneous output.

The same settling time should be observed for the first differential conversion after changing the ADC reference.

2.16.4 Conversion time

Conversion time is the combination of the sampling time and the hold time, usually represented in number of clock cycles. The conversion time is the main parameter in deciding the speed of the ADC.

Also the startup time, sample and hold time and the settling time are all software configurable in ADC's of some high end microcontrollers.

2.17 Sampling rate, throughput rate and bandwidth

Sampling rate is defined as the number of samples converted by the ADC in one second. Bandwidth represents the maximum frequency of the input analog signal that can be given to the ADC. Sampling rate and bandwidth are related by Nyquist sampling theorem. According to this theorem, the sampling rate should be at least twice the bandwidth of the input signal.

Consider the case of single ended conversion where one conversion takes 13 ADC clock cycles. Assuming the ADC clock frequency to be 1MHz, then approximately 77k samples will be converted in one second. That means the sampling rate is 77k. So according to Nyquist theorem, the maximum frequency of the analog input signal is limited to 38.5kHz which represents the bandwidth of the ADC in single ended mode.

Taking the same case above, if 1MHz is the maximum clock frequency that can be applied to an ADC which takes at least 13 ADC clock cycles for converting one sample, then 77k samples per second is said to be the maximum throughput rate of the ADC.

When using differential mode, the bandwidth is limited to few kHz by the internal differential amplifier. So before giving the analog input to the ADC, any frequency components above the mentioned bandwidth should be filtered using external filter to avoid any non-linearity.

2.18 Impedances and capacitances of ADC

Figure 2-19. Equivalent circuit of the ADC system.

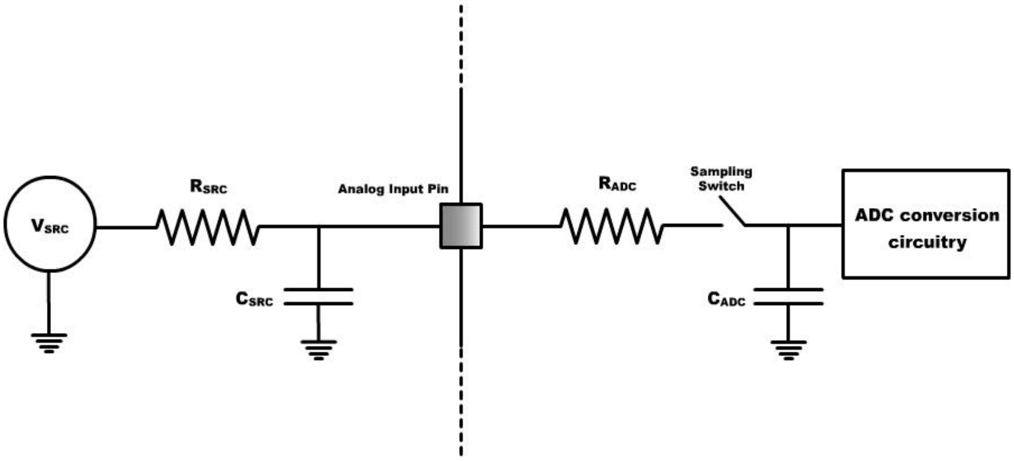


Figure 2-19 depicts the equivalent circuit of ADC system.

Inside the ADC, the sample and hold circuit of the ADC contains a resistance-capacitance (R_{ADC} & C_{ADC}) pair in a low pass filter arrangement. The C_{ADC} is also called as sampling capacitor. Whenever an ADC start conversion signal is issued, the sampling switch, present between the R_{ADC} – C_{ADC} pair, is closed so that the analog input voltage charges the sampling capacitor through the resistance R_{ADC}.

The input impedance of the ADC is the combination of R_{ADC} and the impedance of the capacitor. As the sampling capacitor gets charged to the input voltage, the current through R_{ADC} reduces and ends up with a minimum value when voltage across the sampling capacitor equals the input voltage. So the minimum input impedance of the ADC equals R_{ADC}.

In the source side, the ideal source voltage is subject to some resistance called the source resistance (R_{SRC}) and some capacitance called source capacitance (C_{SRC}) present in the source module. Because of the presence of R_{SRC}, the current entering the sample and hold circuit reduces. So this reduction in current increases the time to charge the sampling capacitance thereby reducing the speed of the ADC. Also the presence of C_{SRC} makes the source to first charge it completely before charging the

sampling capacitor. This reduces the accuracy of the ADC since the sampling capacitor may not be completely charged.

2.19 Oversampling

Oversampling is a process of sampling the analog input signal at a sampling rate significantly higher than the Nyquist sampling rate. The main advantages of oversampling are:

1. It avoids the aliasing problem, since the sampling rate is higher compared to the Nyquist sampling rate.
2. It provides a way of increasing the resolution of the ADC. For example, to implement a 14-bit converter, it is enough to have a 10-bit converter which can run at 256 times the target sampling rate. Averaging a group of 256 consecutive 10-bit samples adds four bits to the resolution of the average, producing a single sample with 14-bit resolution.
3. The number of samples required to get additional n bits is = 2^{2n}.
4. It improves the SNR of the ADC.

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