GENNUM

Using the Gennum Serial Peripheral Interface

GSPI Application Note

Features

HD-Linx® II

- Maximum SCLK speed of 6MHz
- High-impedance SDOUT allows multiple devices to be connected in parallel

Gen-LINX® III

- Maximum SCLK speed of 54MHz
- Auto-increment capability
- Loop-through capability allows multiple devices to be connected in a chain

GEN-Clocks™

- Maximum SCLK speed of 10MHz
- Auto-increment capability
- Loop-through capability allows multiple devices to be connected in a chain

Description

The Gennum Serial Peripheral Interface (GSPI) is a 4-wire interface provided to allow the host to enable additional features and/or to provide additional status information through configuration registers in the device.

The GSPI comprises a serial data input signal SDIN, serial data output signal SDOUT, an active low chip select $\overline{CS}$, and a burst clock SCLK.

Because these pins are shared with the JTAG interface port, an additional control signal pin JTAG/$\overline{HOST}$ is provided. When JTAG/$\overline{HOST}$ is LOW, the GSPI interface is enabled.

When operating in GSPI mode, the SCLK, SDIN, and $\overline{CS}$ signals are provided by the application interface.

The SDOUT pin, for Gen-LINX III and GEN-Clocks devices, may be connected to the SDIN of another device, allowing multiple devices to be connected to the GSPI chain.

The SDOUT pin, for HD-Linx II devices, is a high-impedance output allowing multiple devices to be connected in parallel and selected via the $\overline{CS}$ input.

All read or write access to the GSPI is initiated and terminated by the host processor. Each access always begins with a 16-bit command word on SDIN indicating the address of the register of interest. This is followed by a 16-bit data word on SDIN in write mode, or a 16-bit data word on SDOUT in read mode.

Contents

1. GSPI for HD-Linx II

The Gennum Serial Peripheral Interface, is a 4-wire interface provided to allow the host to enable additional features of the device and /or to provide additional status information through configuration registers in the GSPI.

The GSPI comprises a serial data input signal SDIN, serial data output signal SDOUT, an active low chip select $\overline{CS}$, and a burst clock SCLK. The burst clock must have a duty cycle between 40% and 60%.

Because these pins are shared with the JTAG interface port, an additional control signal pin JTAG/$\overline{HOST}$ is provided. When JTAG/$\overline{HOST}$ is LOW, the GSPI interface is enabled.

When operating in GSPI mode, the SCLK, SDIN, and $\overline{CS}$ signals are provided by the host interface. The SDOUT pin is a high-impedance output allowing multiple devices to be connected in parallel and selected via the $\overline{CS}$ input. The interface is illustrated in Figure 1-1.

All read or write access to the GSPI is initiated and terminated by the host processor. Each access always begins with a 16-bit command word on SDIN indicating the address of the register of interest. This is followed by a 16-bit data word on SDIN in write mode, or a 16-bit data word on SDOUT in read mode.

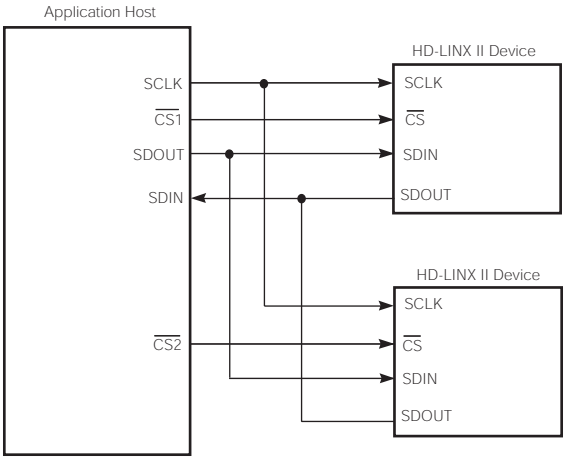

Figure 1-1: HD-Linx II GSPI Application Interface Connection

1.1 Command Word Description

The command word is transmitted MSB first and contains a READ/$\overline{\text{WRITE}}$ bit, nine reserved bits and a 6-bit register address. Set R/$\overline{\text{W}}$ = '1' to read and R/$\overline{\text{W}}$ = '0' to write from the GSPI.

Command words are clocked into the GSPI on the rising edge of the serial clock SCLK. To ensure proper GSPI operation, the timing requirements in Table 1-1 should be followed and each command word must be followed by only one data word.

Figure 1-2: Command Word Format

Figure 1-3: Data Word Format

1.2 Data Read and Write Timing

Read and write mode timing for the GSPI interface is shown in Figure 1-4 and Figure 1-5 respectively. Close up diagrams of the timing are shown in Figure 1-6, Figure 1-7, Figure 1-8, Figure 1-9 and Figure 1-10. The timing parameters are defined in Table 1-1.

When writing to the registers via the GSPI, the MSB of the data word may be presented to SDIN immediately following the falling edge of the LSB of the command word. All SDIN data is sampled on the rising edge of SCLK.

When reading from the registers via the GSPI, the MSB of the data word will be available on SDOUT 12ns following the falling edge of the LSB of the command word, and thus may be read by the host on the very next rising edge of the clock.

Table 1-1: GSPI Timing Parameters

Parameter	Definition	Specification
t_0	The minimum duration of time chip select, $\overline{\text{CS}}$, must be LOW before the first SCLK rising edge. (See Figure 1-6)	1.5 ns
t_1	On-time tolerated by SCLK. (See Figure 1-7)	40% to 60%
t_2	The minimum SCLK period. (See Figure 1-7)	166.7 ns
t_3	Minimum input setup time. (See Figure 1-8)	0 s
t_4	Minimum input hold time. (See Figure 1-8)	1.43 ns

Table 1-1: GSPI Timing Parameters (Continued)

Parameter	Definition	Specification
t_5	Minimum output hold time. (See Figure 1-9)	1.5 ns
t_6	Maximum output data delay time. (See Figure 1-9)	7.27 ns
t_7	Time between the falling edge of the LSB of the command word and the availability of the MSB of the data word. (See Figure 1-10)	12 ns

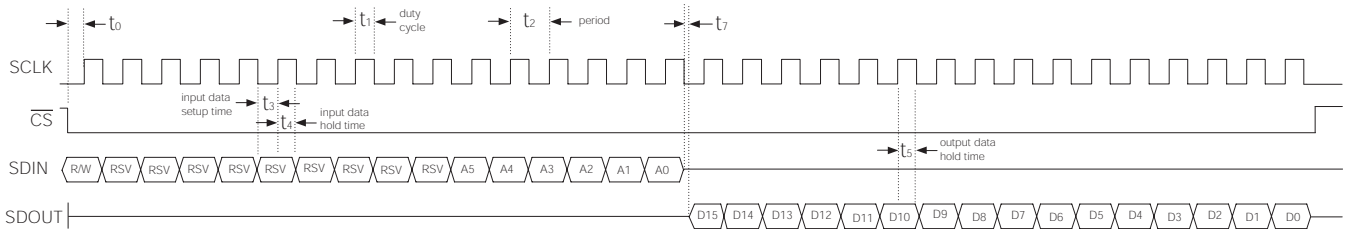

Figure 1-4: GSPI Read Mode Timing

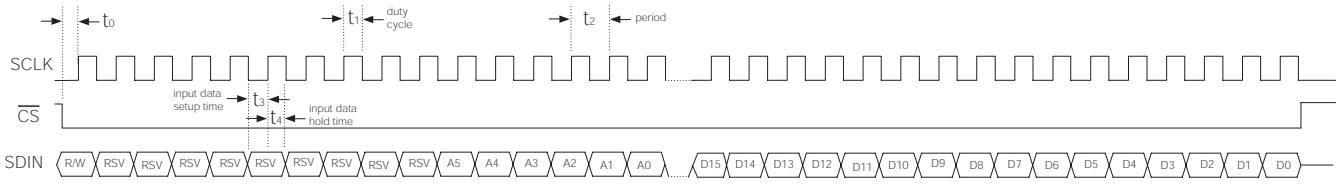

Figure 1-5: GSPI Write Mode Timing

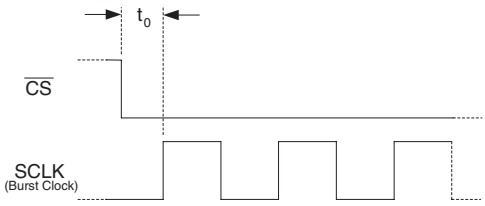

Figure 1-6: $\overline{CS}$ Timing

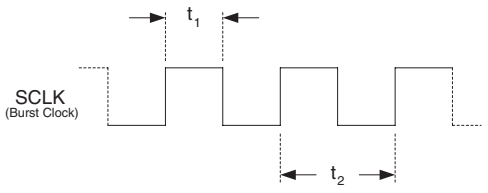

Figure 1-7: SCLK Timing

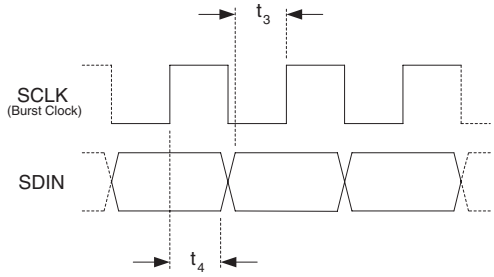

Figure 1-8: SDIN Timing

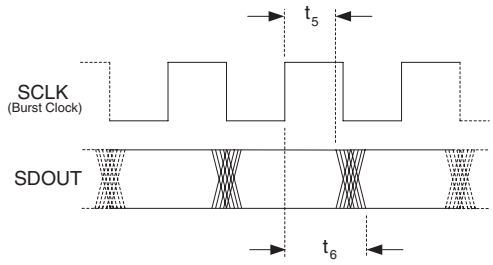

Figure 1-9: SDOUT Timing

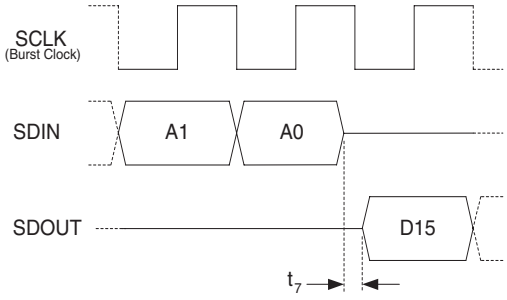

Figure 1-10: Command Word to Data Word Timing

2. GSPI for Gen-LINX III and GEN-Clocks

The Gennum Serial Peripheral Interface, is a 4-wire interface provided to allow the host to enable additional features and/or to provide additional status information through configuration registers in the device.

The GSPI comprises a serial data input signal SDIN, serial data output signal SDOUT, an active low chip select $\overline{CS}$, and a burst clock SCLK.

Because these pins are shared with the JTAG interface port, an additional control signal pin JTAG/$\overline{HOST}$ is provided. When JTAG/$\overline{HOST}$ is LOW, the GSPI interface is enabled.

When operating in GSPI mode, the SCLK, SDIN, and $\overline{CS}$ signals are provided by the application interface. The SDOUT pin may be connected to the SDIN of another device, allowing multiple devices to be connected to the GSPI chain. The interface is illustrated in Figure 2-1.

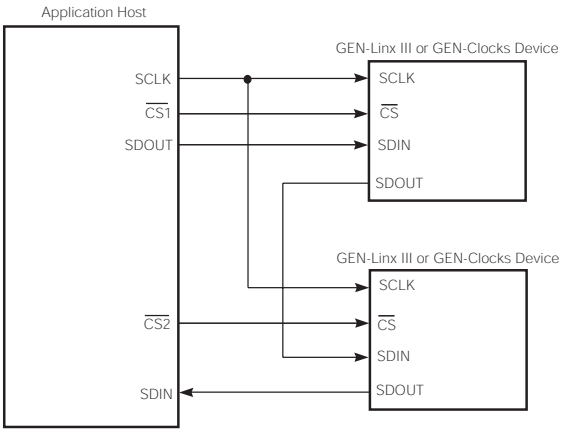

Figure 2-1: Gen-LINX III and GEN-Clocks GSPI Application Interface Connection

All read or write access to the device is initiated and terminated by the host processor. Each access always begins with a 16-bit command word on SDIN indicating the address of the register of interest. This is followed by a 16-bit data word on SDIN in write mode, or a 16-bit data word on SDOUT in read mode.

2.1 Command Word Description

The command word consists of a 16-bit word transmitted MSB first and contains a READ/$\overline{\text{WRITE}}$ bit, an Auto-Increment bit and a 12-bit address. Figure 2-2 shows the command word format and bit configurations.

Command words are clocked into the device on the rising edge of the serial clock SCLK, which operates in a burst fashion.

When the Auto-Increment bit is set LOW, each command word must be followed by only one data word to ensure proper operation. If the Auto-Increment bit is set HIGH, the following data word will be written into the address specified in the command word, and subsequent data words will be written into incremental addresses from the previous data word. This facilitates multiple address writes without sending a command word for each data word.

Auto-Increment may be used for both read and write access.

Auto-Increment is terminated when $\overline{\text{CS}}$ is deasserted ($\overline{\text{CS}}$ = LOW-to-HIGH).

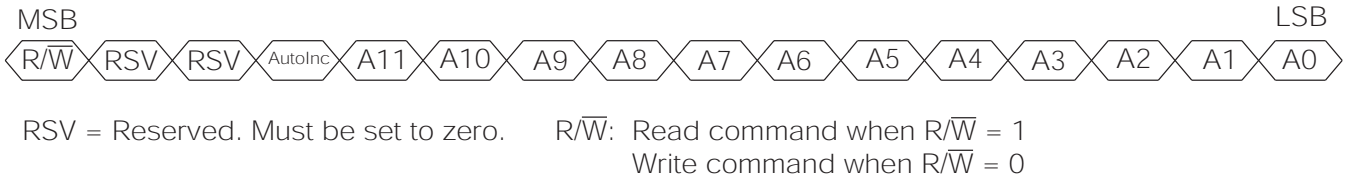

Figure 2-2: Command Word Format

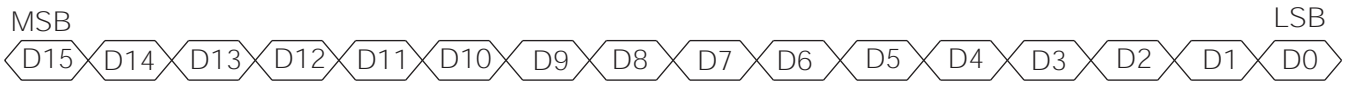

Figure 2-3: Data Word Format

2.2 Data Read and Write Timing

Read and write mode timing for the GSPI interface is shown in Figure 2-4 and Figure 2-5 respectively. Close up diagrams of the timing are shown in Figure 2-6, Figure 2-7, Figure 2-8 and Figure 2-9. The timing parameters are defined in Table 2-1.

When several devices are connected to the GSPI chain, only one $\overline{CS}$ must be asserted during a read sequence.

During the write sequence, all command and following data words input at the SDIN pin are output at the SDOUT pin as is. Where several devices are connected to the GSPI chain, data can be written simultaneously to all the devices that have $\overline{CS}$ set LOW.

Table 2-1: GSPI Timing Parameters

Parameter	Definition	Specification
t_0	The minimum duration of time chip select, $\overline{CS}$, must be LOW before the first SCLK rising edge. (See Figure 2-6)	1.5 ns
t_1	The minimum SCLK period. (Gen-LINX III devices) (See Figure 2-7)	18.5 ns
	The minimum SCLK period. (GEN-Clocks devices) (See Figure 2-7)	100 ns
t_2	On-time tolerated by SCLK. (See Figure 2-7)	40% to 60%
t_3	Minimum input setup time. (See Figure 2-8)	1.5 ns
t_4	Write Cycle: the minimum duration of time between the last SCLK command (or data word if the Auto-Increment bit is HIGH) and the first SCLK of the data word. (See Figure 2-5)	37.1 ns
t_5	Read Cycle: the minimum duration of time between the last SCLK command (or data word if the Auto-Increment bit is HIGH) and the first SCLK of the data word. (See Figure 2-4)	148.4 ns
	Read Cycle - FIFO in ANC Extraction Mode: the minimum duration of time between the last SCLK command (or data word if the Auto-Increment bit is HIGH) and the first SCLK of the data word. (Gen-LINX III devices only) (See Figure 2-4)	222.6 ns
t_6	Minimum output hold time. (See Figure 2-9)	1.5 ns
t_7	The minimum duration of time between the last SCLK of the GSPI transaction and when $\overline{CS}$ can be set HIGH. (See Figure 2-5)	37.1 ns
t_8	Minimum input hold time. (See Figure 2-8)	1.5 ns

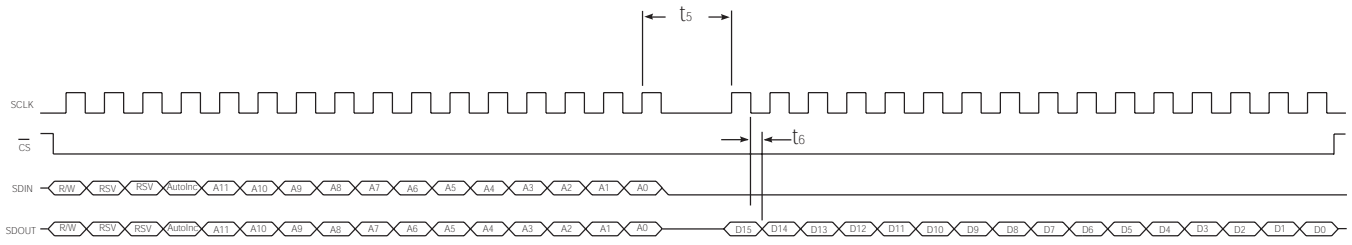

Figure 2-4: GSPI Read Mode Timing

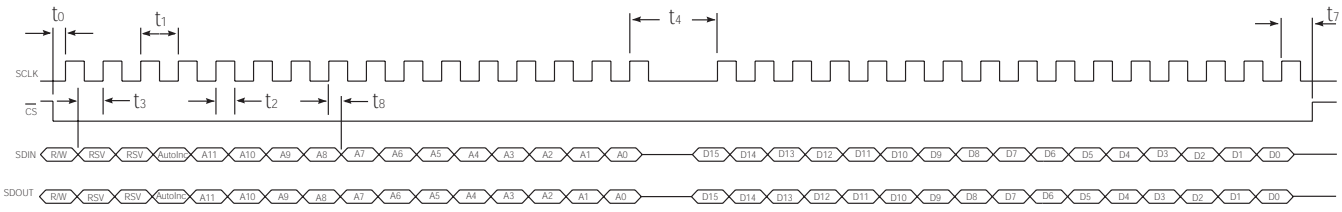

Figure 2-5: GSPI Write Mode Timing

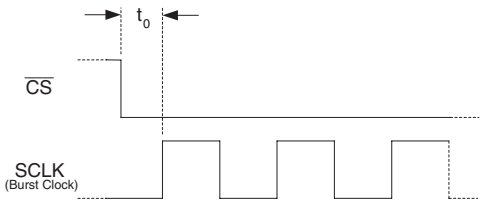

Figure 2-6: $\overline{CS}$ Timing

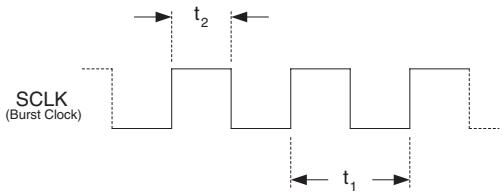

Figure 2-7: SCLK Timing

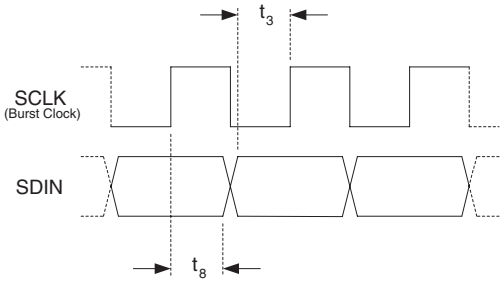

Figure 2-8: SDIN Timing

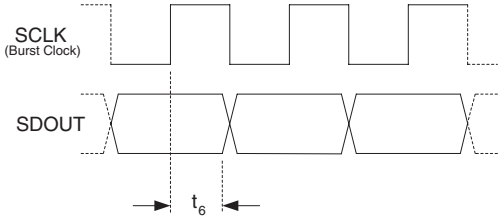

Figure 2-9: SDOUT Timing

3. Revision History

Version	ECR	Date	Changes and/or Modifications
0	136511	May 2005	New Document.

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GENNUM CORPORATION
Mailing Address: P.O. Box 489, Stn. A, Burlington, Ontario, Canada L7R 3Y3
Shipping Address: 970 Fraser Drive, Burlington, Ontario, Canada L7L 5P5
Tel. +1 (905) 632-2996 Fax. +1 (905) 632-5946

GENNUM JAPAN CORPORATION
Shinjuku Green Tower Building 27F, 6-14-1, Nishi Shinjuku, Shinjuku-ku, Tokyo, 160-0023 Japan
Tel. +81 (03) 3349-5501, Fax. +81 (03) 3349-5505

GENNUM UK LIMITED
25 Long Garden Walk, Farnham, Surrey, England GU9 7HX
Tel. +44 (0)1252 747 000 Fax +44 (0)1252 726 523

www.gennum.com