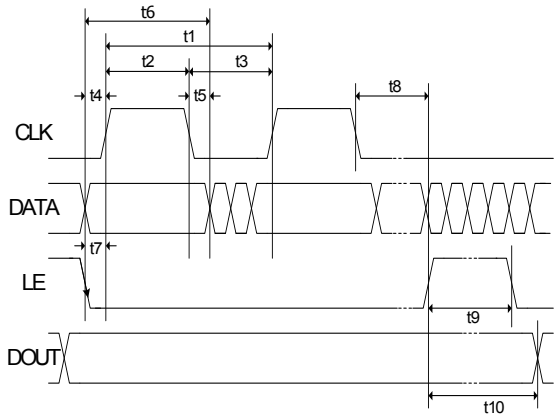
Truth Table

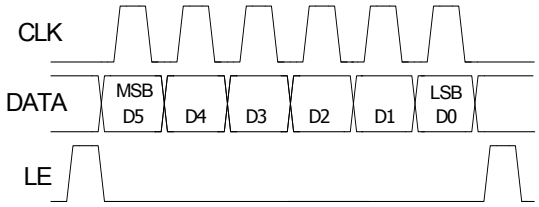
Control Bit						Gain Relative to Maximum Gain
D5	D4	D3	D2	D1	D0	
1	1	1	1	1	1	0dB
1	1	1	1	1	0	-0.5dB
1	1	1	1	0	1	-1dB
1	1	1	0	1	1	-2dB
1	1	0	1	1	1	-4dB
1	0	1	1	1	1	-8dB
0	1	1	1	1	1	-16dB
0	0	0	0	0	0	-31.5dB

Serial Port Interface:

SPI Timing Diagram



Programming example - 6-bit



Specifications: SPI Timing Diagram

Parameter	Limit	Unit	Comment
t1	25	MHz max	CLK Frequency
t2	20	ns min	CLK High
t3	20	ns min	CLK Low
t4	5	ns min	DATA to CLK Setup Time
t5	5	ns min	DATA to CLK Hold Time
t6	30	ns min	DATA Valid
t7	5	ns min	LE to CLK Setup Time
t8	5	ns min	CLK to LE Setup Time
t9	10	ns min	LE Pulse Width
t10	20	ns max	Output Set

Control Voltage Table		
State	V_{DD} = +3V	V_{DD} = +5V
Low	0V to 0.8V	0V to 0.8V
High	2.0 to V_{DD}	2.0 to V_{DD}

Power-up Programming Truth Table	
PUP	Attenuator Setting
Low	Attenuation at Max, 31.5dB
High	Attenuation at Min, 0dB

7628 Thorndike Road, Greensboro, NC 27409-9421 · For sales or technical support, contact RFMD at (+1) 336-678-5570 or customerservice@rfmd.com.