

Automotive Line Transient Protection Circuit

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ABSTRACT

Automobile electrical power systems are subjected to many tortuous conditions over the life of the vehicle. In addition to adverse conditions on the battery power bus, there are also operating extremes due to environmental factors such as temperature, humidity and long term vehicle storage. This application note will discuss how these transient conditions are formed and the design requirements for the circuit to protect electrical systems down the line.

Contents

1	TRANSIENTS IN AUTOMOTIVE APPLICATIONS.....	1
2	DESIGN REQUIREMENTS	2
2.1	Quiescent Current	2
2.2	Polarity Guard	2
2.3	Overvoltage Protection and Supervisory Circuit	3
2.4	Overall Circuit Parameters.....	4
3	FUNCTIONAL BLOCK DIAGRAM.....	4
4	AUTOMOTIVE LINE TRANSIENT PROTECTION CIRCUIT SCHEMATIC.....	5
5	CIRCUIT DESCRIPTION	6
5.1	Reverse Polarity Protection and Overvoltage Disconnect.....	6
5.2	Soft-Start and Inrush Control	7
5.3	SMPS Enable Supervisory Circuit	8
6	TEST SETUP AND CONNECTIONS	9
7	TYPICAL PERFORMANCE CURVES.....	10
8	BILL OF MATERIALS.....	12

1 TRANSIENTS IN AUTOMOTIVE APPLICATIONS

While the vehicle battery is capable of large currents for re-starting the engine and serves as a reservoir for high power accessories such as headlights, blowers and cigarette lighters; the voltage level is poorly regulated even in the best operating conditions. Fault conditions make matters even worse. Open battery cells (or a dirty battery terminal) will lead to a “load dump” if an open battery event occurs while the vehicle engine is running. A load dump event creates a surge voltage to the 12 V vehicle bus that reaches 40 V to 60 V for a short period of time.

Other physical factors in vehicle design are also a concern. In particular there are long power supply lines that feed from the power distribution box in the engine compartment to the distant corners of the vehicle. Because of the inductive characteristic of long leads there are even higher transient levels than those that occur during load dump. The governing specification for tail light electronics is that they be able to withstand transients of +100 V and -300 V. This is a foreboding challenge for IC based electronics such as LED tail light regulators.

2 DESIGN REQUIREMENTS

2.1 Quiescent Current

A typical 12 V lead acid battery based vehicle power system has a very high current capability primarily because a starter motor must be able to turn the vehicle engine over each time the engine is to be re-started. The engine starting event may occur many times during the course of a day and as infrequently as once in several weeks. Thus it is important that all electronic systems attached directly to the battery bus have the lowest possible quiescent (or operating) current while the vehicle is shut-down and not charging so that the periods of nonoperation can be as long as possible. This low quiescent current requirement is also true of added protection circuits.

With these factors in mind, a combination of discrete devices can be assembled to create a low quiescent current, self-resetting protection circuit. This circuitry will allow survival of a typical IC based switching mode dc-dc converter that would otherwise be damaged by input voltages outside of its operating ratings.

2.2 Polarity Guard

The first electrical function of a protection system is that of a polarity guard. A polarity guard prevents circuit damage due to application of negative polarity input voltage. Reverse polarity source voltage occurs due to either normal wiring inductance transients or from the accidental reversal of battery terminals during vehicle battery replacement or dead battery jump starting. Thus this stage of the protection system is that of a reverse input polarity protection mechanism. In normal operation the stage passes the input voltage directly through and should have the lowest practical forward voltage drop. Finite voltage drop results in lowering the dropout headroom of the protected downstream electrical circuitry. So a leading motive in polarity guard design is to migrate toward a circuit with the lowest forward drop. A polarity guard using a MOSFET would appear to be the best choice as it offers the lowest drop of the available choices.

In contrast to the requirement of low forward voltage drop during normal operation is the opposing requirement that during the reversed input voltage blocking state the breakdown rating may need to stand off several hundreds of volts without damage. In this case a silicon diode would be the best choice due to the limited breakdown rating of available schottky diodes, usually 100V maximum. A tradeoff is that conventional silicon diodes have the highest forward drop during normal system operation.

There is a third less obvious function of the polarity guard stage. The downstream protected circuit section may include sizable bulk capacitance as part of its design requirements. During normal operation this bulk storage capacitance will be charged to approximately the power bus rail voltage. There can then be fault conditions whereby the input voltage bus is temporarily and rapidly shorted to ground. Such an event can occur if jumper cables on a running system are momentarily tapped together. If such an event occurs, the downstream bulk capacitance might then be discharged out through the input and cause a surge of current that may damage related circuitry. To prevent this reverse action, the polarity guard should exhibit diode blocking action during such an event. This blocking characteristic cannot be achieved with a simple MOSFET approach as it conducts in either direction when enhanced. It might be possible to create a MOSFET controller that could resolve this limitation but it would require quiescent current for operation.

In summary, diodes are simple, low cost, two terminal devices which provide the added benefit of preventing reverse current flow from charged bulk capacitors within the protected stage. There is the further factor that high voltage P-channel MOSFETS are comparatively expensive and if they are to be considered, then search for a solution where as few as possible are employed.

[Figure 1](#) and [Figure 2](#) show three contending polarity guard approaches. During normal operation below 18 V all three approaches require no bias current for operation. In the case of the two diode ([Figure 1](#)) approaches this should be obvious as they are floating two terminal applications that have no path to ground. In the case of the p-channel mosfet ([Figure 2](#)) there is no gate current flow just leakage current through the zener diode gate protection clamp.

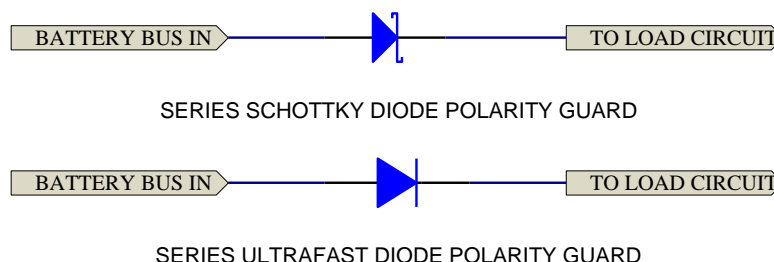


Figure 1. Diode Polarity Guard

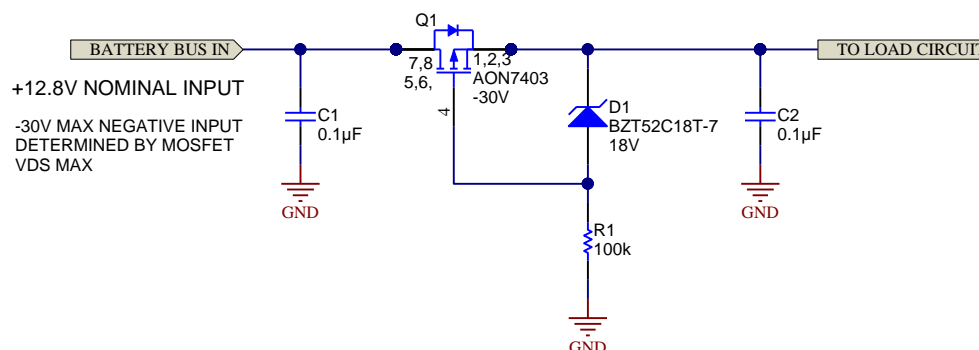


Figure 2. PFET Polarity Guard

The first two options in [Figure 1](#) are simple diode based blocks that differ in the choice of diode type, either Schottky with lowest available forward voltage drop, or a more conventional silicon diode type that has higher forward voltage drop. The advantage of using the higher drop silicon selection is a much lower cost and higher maximum reverse voltage rating. Schottky diode maximum reverse voltage ratings generally top out at 100 V. In contrast silicon diodes are available as high as 600 V or even greater. As previously mentioned, the diode forward voltage drop during normal system operation is a system power loss contributor, so forward voltage drop should be minimized. If the higher forward drop of silicon diode is permissible, then it is the best economic choice. These are much lower in cost than equivalent Schottky based diodes and have multiple vendor choices. In this blocking application the speed of the diode is not a concern at all, but in comparing diode characteristics it is observed that faster diodes generally have lower forward drop. Following this comparison of available diodes and their tradeoffs, it is suggested that the leading choice for a low drop high voltage diode would be those in the Ultra-Fast recovery category.

2.3 Overvoltage Protection and Supervisory Circuit

The next element in the protection circuit is an overvoltage disconnect switch. For simplicity, a p-channel MOSFET is selected. As previously mentioned; these are not low cost devices. However, this choice comes with a benefit of not needing an extra gate supply voltage for bias as would be the case if an n-channel MOSFET were chosen. Therefore the idea is that the added cost of using a p-channel will outweigh the extra additional circuitry required to drive an n-channel. Additionally this leads to an overall solution with essentially zero standby current. The p-channel series switch can also perform a soft-start function by adding two R-C networks. This allows “hot connecting” large capacitive loads without “sparking”. Be aware that optimum performance of this surge limit function involves calculations based on load capacitor value and MOSFET capacitance characteristics

Finally, it is desirable to place a supervisor across the series p-channel switch such that the protected load is only enabled when the switch is fully conducting.

2.4 Overall Circuit Parameters

Figure 4 shows the full circuit schematic of the design. Considering all of the above requirements, this resulting circuit has:

1. Essentially zero operating current during normal operation as the only conducting semiconductor in this mode is the p-channel MOSFET.
2. Programmable over-voltage disconnect determined by selection of zener diodes.
3. Programmable in-rush current based on two R-C networks in conjunction with MOSFET and bulk input capacitor calculations.
4. Immunity to damage in the event of a shorted input bus during operation.
5. OVP that self-resets when input voltage returns to normal operating range.
6. Does not rely on dissipative limiting.
7. Does not blow fuses when in voltage limiting mode.

3 FUNCTIONAL BLOCK DIAGRAM

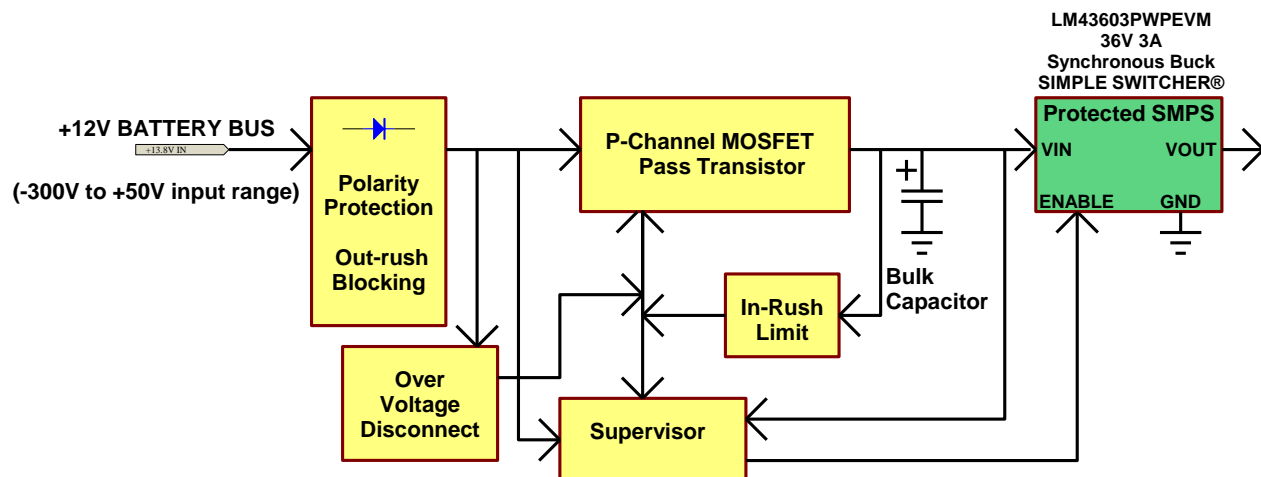


Figure 3. Functional Block Diagram for the Automotive Input Protection Circuit

4 AUTOMOTIVE LINE TRANSIENT PROTECTION CIRCUIT SCHEMATIC

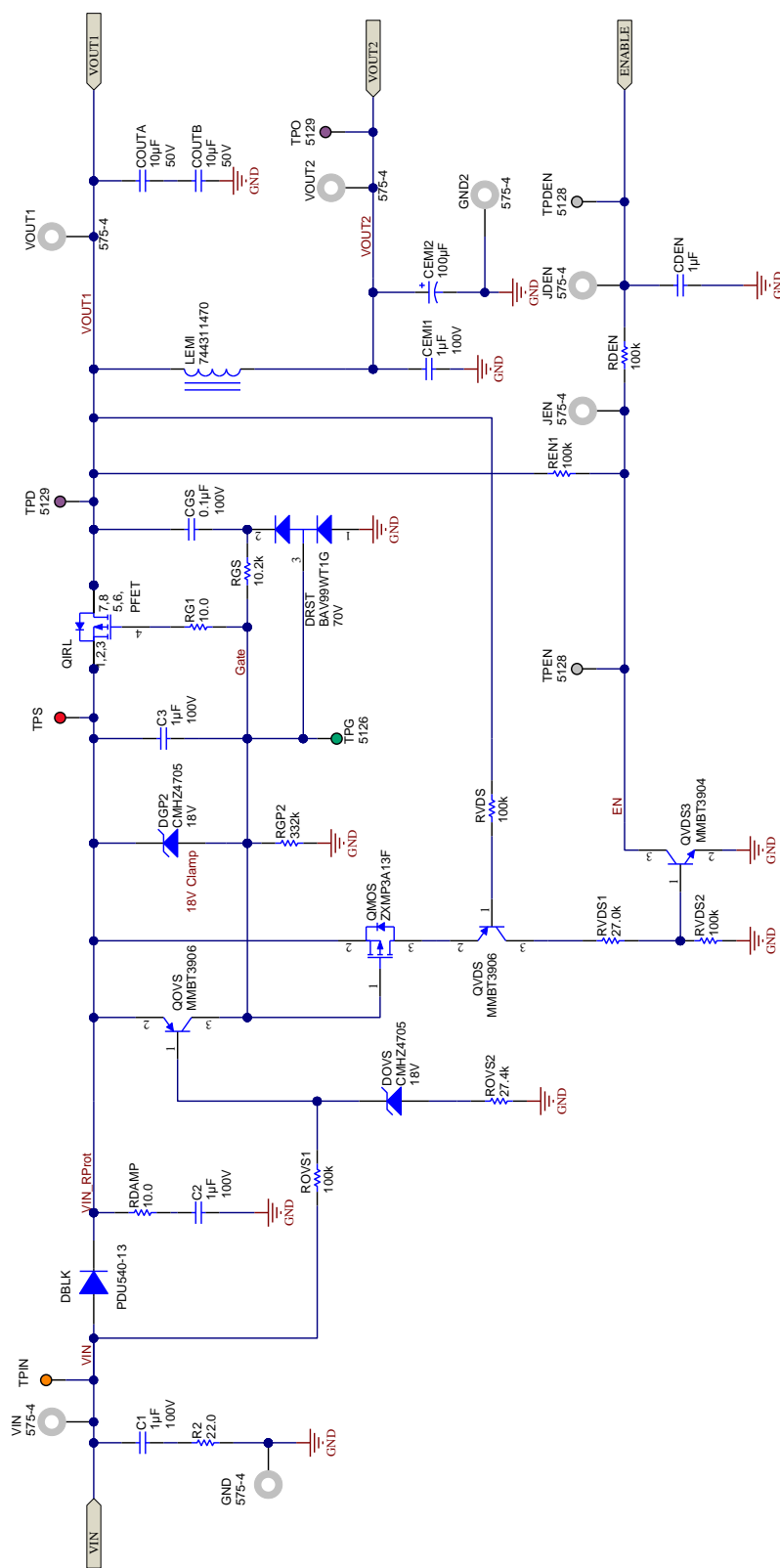


Figure 4. Automotive Line Transient Protection Circuit Schematic

5 CIRCUIT DESCRIPTION

5.1 Reverse Polarity Protection and Overvoltage Disconnect

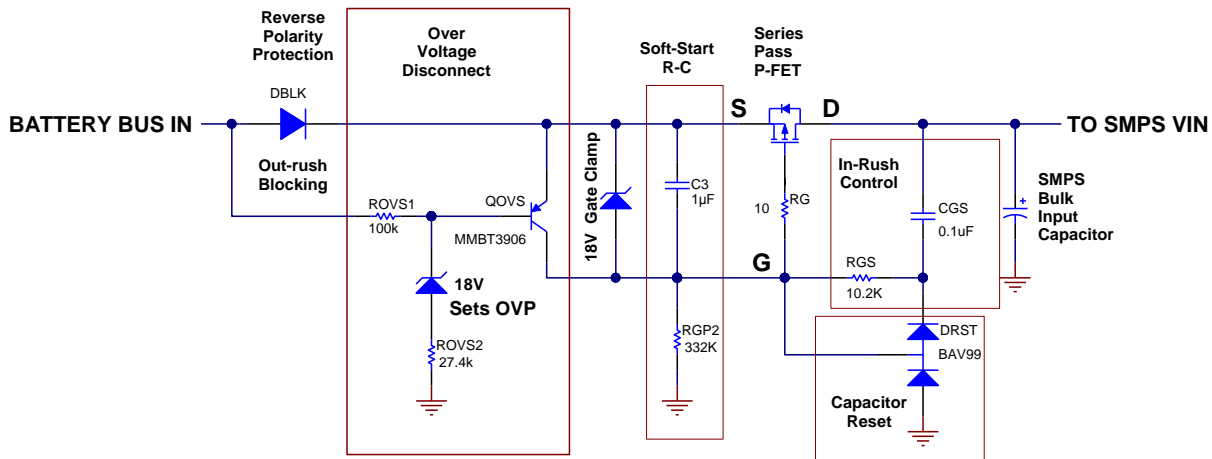


Figure 5. Soft-Start and Protection Circuit

The component ROVS1, QOVS and the zener diode in Figure 5 set the OVP voltage level at the circuit input. Initially when the input voltage is below 18 V, the QOVS transistor will be in an off state allowing the capacitor C3 to be charged through C3 and RGP2 thus turning on the PFET. Once the input voltage reaches approximately 18V plus 2 diode drops, the transistor QOVS will be turned on since the base of QOVS is held at the zener voltage of 18 V. When this transistor is turned on, it discharges capacitor C3 and pulls the gate of PFET to its source and thus turning the PFET OFF.

Once the input voltage goes back below 18 V, the OVP condition is cleared and QOVS is again turned off. This allow the capacitor C3 to be slowly charged again, resulting a soft-start at the output. The whole OVP sequence can be seen on Figure 6. Please refer to Figure 10 for test setup.

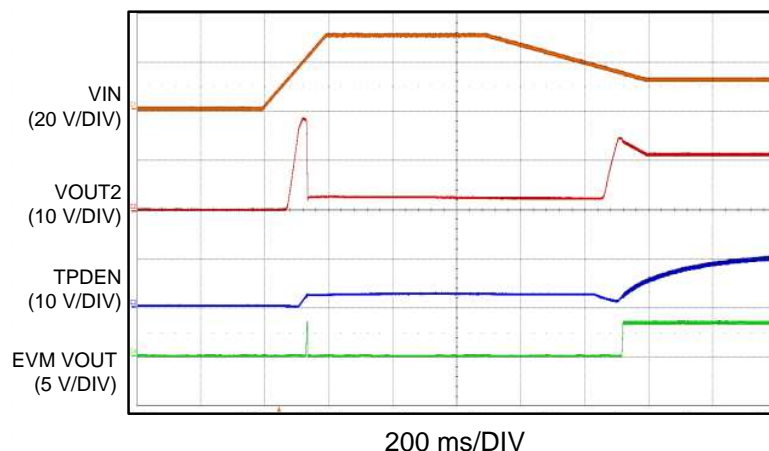


Figure 6. 30V OVP Condition and Recovering from OVP at 12V

The Ultrafast diode (DBLK) in Figure 5 is used to block a negative voltage at the battery bus input. During negative transition of the input voltage, the QOVS is also turned on to discharge the capacitor C3. The discharging of the capacitor is required in order to ensure that soft-start is being implemented on the PFET after the input voltage recovers from negative transition. Figure 7 shows the soft-start at VOUT2 after every negative transition at the input. Also, there is a delayed enable response (TPDEN) for downstream circuitry in order to make sure that the PFET is fully turned on before enabling the SMPS.

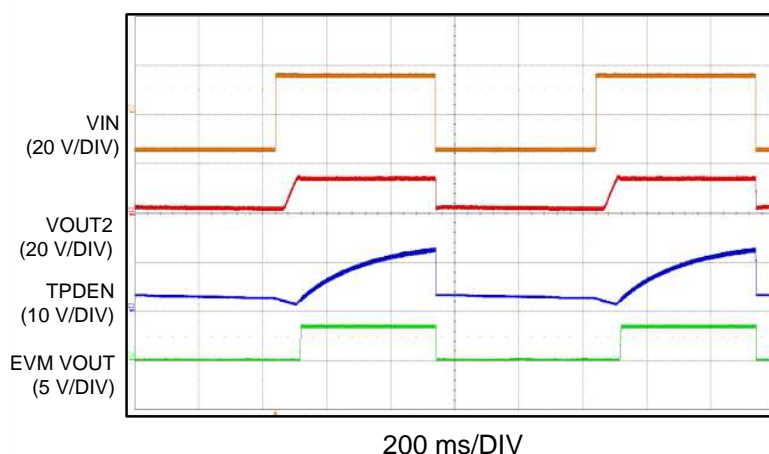


Figure 7. +15 V to -15 V Transition at the input and soft-start at VOUT2

5.2 Soft-Start and Inrush Control Circuit

Referring to [Figure 5](#), C3 and RGP2 alongside with CGS and RGS components are responsible for the soft-start and inrush limit for the PFET. Initially the voltage across capacitor C3 is 0 V. Once the battery is connected, the capacitor will charge towards the battery bus voltage with a pre-determined rate set by the value of C3 and RGP2. The component CGS and RGS are used as a feedback network from drain to gate of the PFET. If the drain voltage of the PFET rises too fast, then this voltage will couple back into the gate of the PFET through CGS and RGS and slows down the rise time of the drain. By soft-starting the PFET, the inrush current going to the bulk capacitors at the output will then be reduced. [Figure 8](#) shows the PFET gate transition during soft-start of the output.

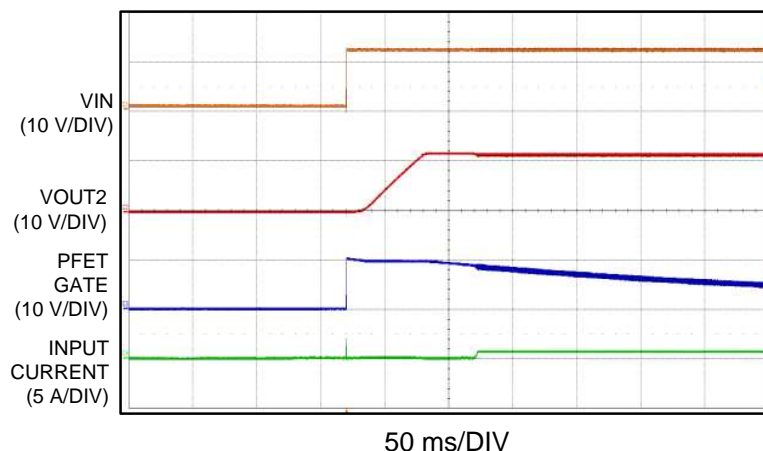


Figure 8. PFET gate transition during soft-start

5.3 SMPS Enable Supervisory Circuit

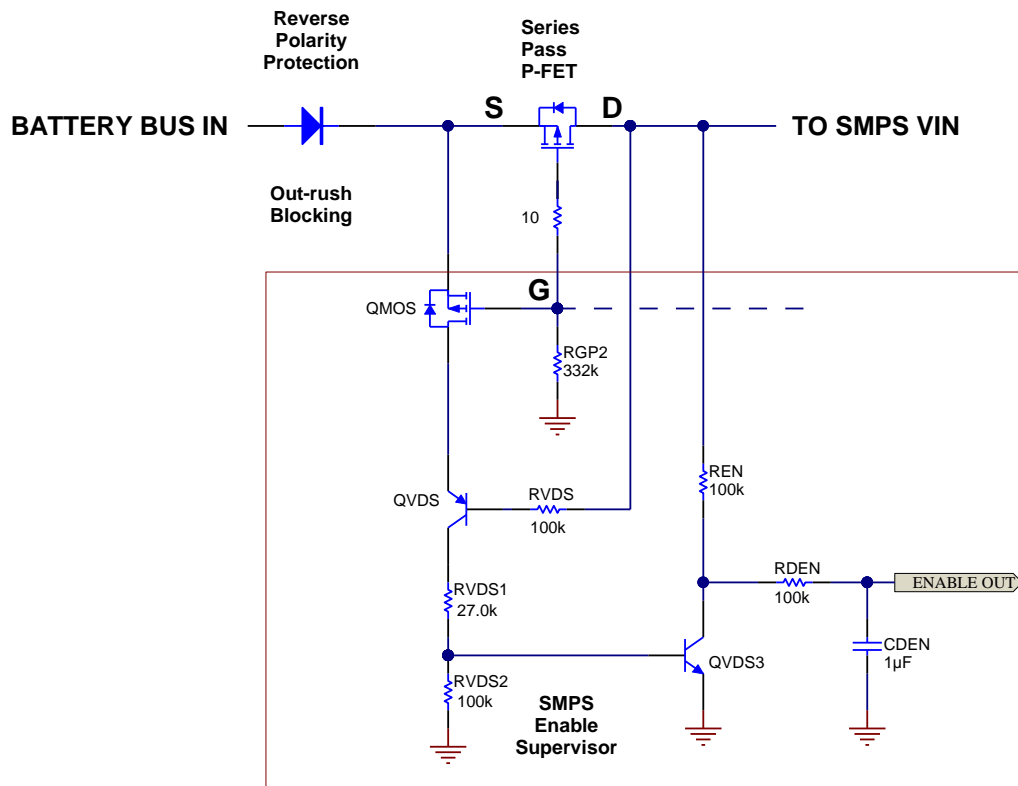


Figure 9. SMPS Enable Supervisory Circuit

Figure 9 shows the enable supervisory section of the circuit. This circuitry monitors the voltage across the drain and source of the PFET to determine whether or not the PFET is fully turned on. Initially the QMOS is on and QVDS monitors the voltage across the source and drain of the PFET. When the PFET is not fully turned on, there is a voltage drop between source and drain of the FET. When this voltage is large enough, then the QVDS will be turned on and pulled up to the PFET source. This voltage will then drive the QVDS3 causing Enable Out node to be pulled low. The ENABLE OUT node can be used to disable the downstream circuitry that has an enable pin to start-up. Therefore the current should not flow into the protected circuitry without the PFET being fully turned on. When the PFET is fully on, QVDS will be turned off and the Enable Out node will slowly rise towards SMPS VIN voltage with a rate determined by RDEN and CDEN.

During input over-voltage events, the QMOS transistor is off due to QOVS being on which makes $V_{GS} = 0$. When QMOS is off, the current path through QVDS and RVDS is opened and removed as a shunt path across the series pass PFET

RDEN and CDEN create a delayed Enable signal to allow more time for the series pass PFET to be turned fully on in the initial startup. Additionally it acts as a delayed turn-off in the OVP state to maintain SMPS operation to discharge the bulk CIN and reset the two R-C networks on the PFET.

6 TEST SETUP AND CONNECTIONS

Throughout the dynamic testing of the Automotive Line Transient Protection Circuit (Figure 13 to Figure 18), a LM43603PWPEVM is attached at the VOUT2 and the TPDEN is connected to the EN post on the EVM. The EVM itself is operating with a set output voltage of 3.3 V and a switching frequency of 500 kHz.

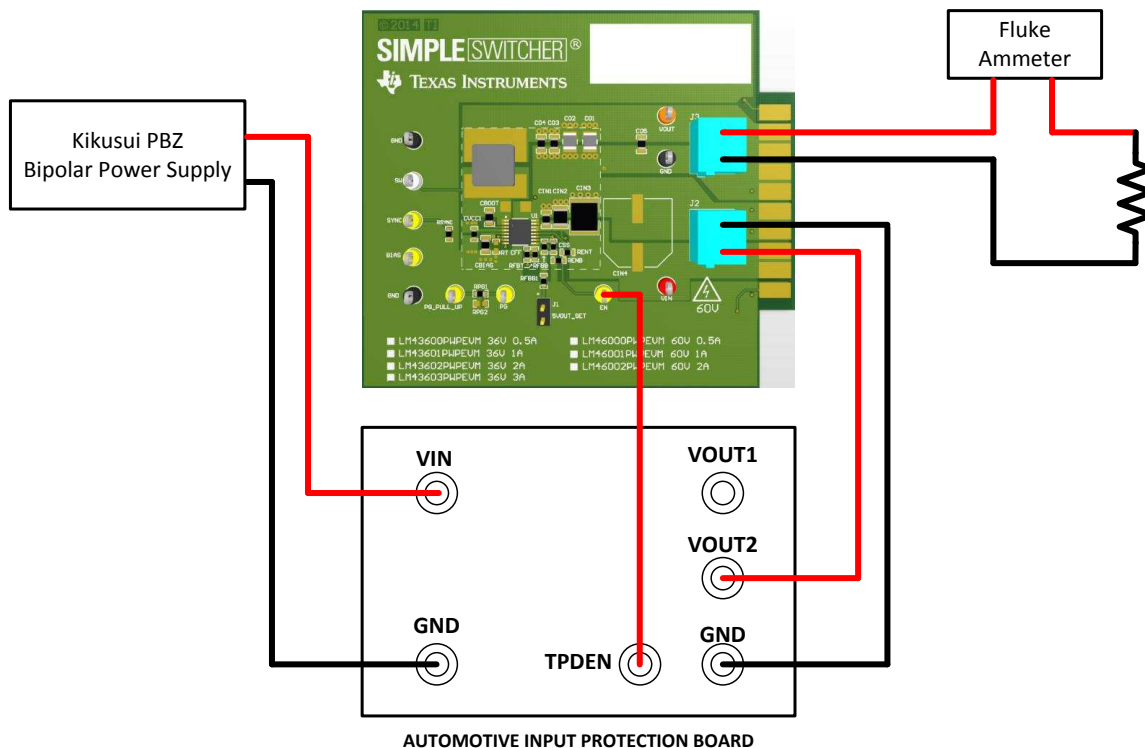


Figure 10. Test Setup and Connection for Automotive Input Protection Circuit

7 TYPICAL PERFORMANCE CURVES

All the curves below are taken with the LM43603PWPEVM attached at the output of the Automotive Input Protection Board. The EVM operating conditions are $V_{OUT} = 3.3\text{ V}$, $F_s = 500\text{ kHz}$, and 1.1 Ohm Load .

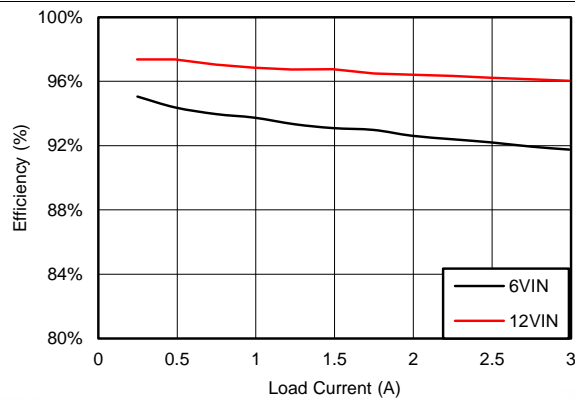


Figure 11. Efficiency

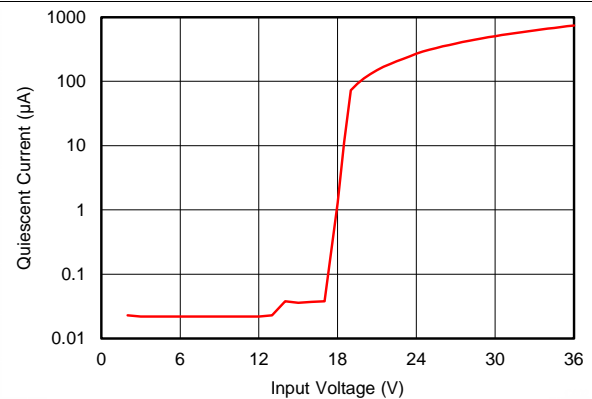


Figure 12. Quiescent Current vs VIN

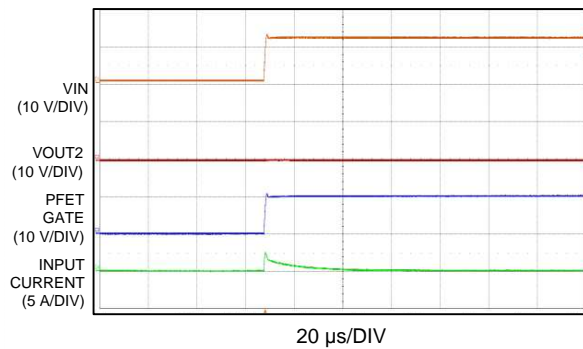


Figure 13. Initial Inrush Current at 12 V Input Hot-Swap

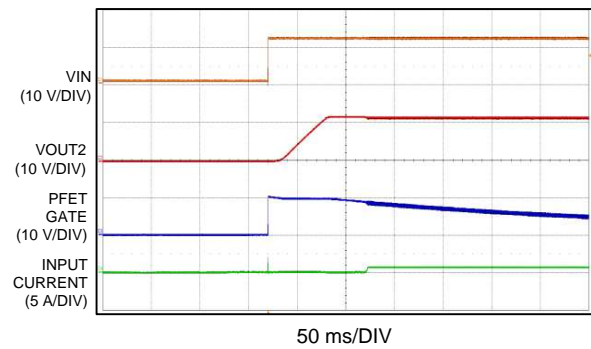


Figure 14. PFET Gate Transition after 12 V Input Hot-Swap

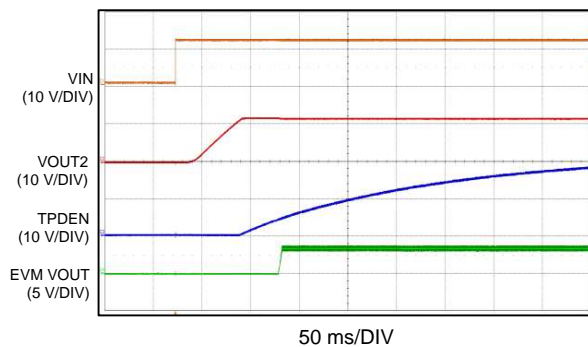


Figure 15. Delayed Enabled Response (TPDEN) for downstream circuitry after Hot-Swap

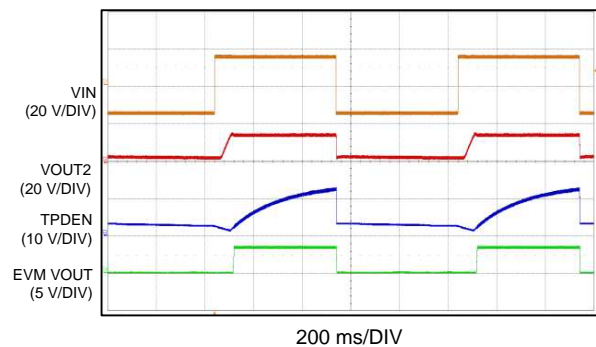


Figure 16. Soft Start on VOUT2 after multiple +15 V to -15 V Input Transition

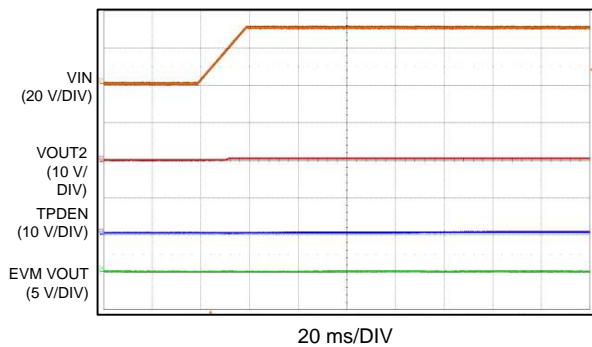


Figure 17. OVP at 30 V Input with 20 ms ramp

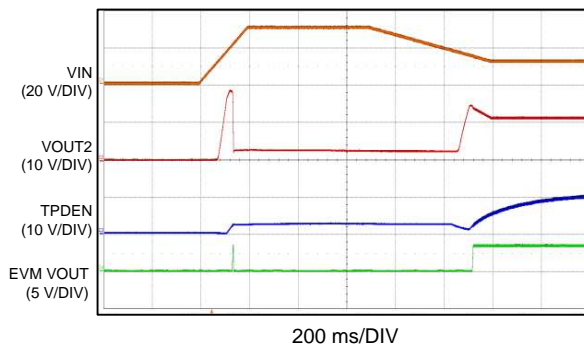


Figure 18. OVP at 30 V Input and Recovery from OVP

8 BILL OF MATERIALS

Table 1. Bill of Materials (BOM) for Automotive Input Protection Board

Designator	Description	Manufacturer	PartNumber	Quantity
C1, C2, C3, CDEN, CEMI1	CAP, CERM, 1uF, 100V, +/-10%, X7R, 1206	MuRata	GRM31CR72A105KA01L	5
CEMI2	CAP, AL, 100uF, 50V, +/-20%, 0.3 ohm, SMD	Panasonic	EEE-FC1H101P	1
CGS	CAP, CERM, 0.1uF, 100V, +/-10%, X7R, 1206	MuRata	GRM319R72A104KA01D	1
COUTA, COUTB	CAP, CERM, 10uF, 50V, +/-10%, X5R, 1206_190	TDK	CGA5L3X5R1H106K160AB	1
DBLK	Diode, Ultrafast Recovery Rectifier, 400V, 5A, PowerDI-5	Diodes Incorporated	PDU540-13	1
DGP2, DOVS	Diode, Zener, 18V, 500mW, SOD-123	Central Semiconductor	CMHZ4705	2
DRST	Diode, P-N, 70V, 0.2A, SOT-323	Fairchild Semiconductor	BAV99WT1G	1
GND, GND2, JDEN, JEN, VIN, VOUT1, VOUT2	Standard Banana Jack, Uninsulated, 5.5mm	Keystone	575-4	7
LEMI	Shielded Drum Core, Superflux, 4.7uH, 6A, 0.02 ohm, SMD	Würth Elektronik eiSos	744311470	1
QIRL	MOSFET, P-Channel, -60V, -42A, 0.025 ohm, TO-220AB	Vishay-Siliconix	SUP53P06-20	1
QMOS	MOSFET, P-Channel, -30V, -1.6A, 0.21 ohm, SOT-23	Diodes Incorporated	ZXMP3A13F	1
QOVS, QVDS	Transistor, PNP, 40V, 0.2A, SOT-23	Fairchild Semiconductor	MMBT3906	2
QVDS3	Transistor, NPN, 40V, 0.2A, SOT-23	Fairchild Semiconductor	MMBT3904	1
R2	RES, 22.0 ohm, 1%, 0.25W, 1206	Yageo America	RC1206FR-0722RL	1
RDAMP, RG1	RES, 10.0 ohm, 1%, 0.25W, 1206	Vishay-Dale	CRCW120610R0FKEA	1
RDEN, REN1, ROVS1, RVDS, RVDS2	RES, 100k ohm, 1%, 0.25W, 1206	Vishay-Dale	CRCW1206100KFKEA	5
RGP2	RES, 332k ohm, 1%, 0.25W, 1206	Yageo America	RC1206FR-07332KL	1
RGS	RES, 10.2k ohm, 1%, 0.25W, 1206	Vishay-Dale	CRCW120610K2FKEA	1
ROVS2, RVDS1	RES, 27.0k ohm, 1%, 0.25W, 1206	Yageo America	RC1206FR-0727KL	1
TPD, TPO	Test Point, Multipurpose, Purple, TH	Keystone	5129	1
TPDEN, TPEN	Test Point, Multipurpose, Grey, TH	Keystone	5128	1
TPG	Test Point, Multipurpose, Green, TH	Keystone	5126	1
TPIN	Test Point, Multipurpose, Orange, TH	Keystone	5013	1
TPS	Test Point, Multipurpose, Red, TH	Keystone	5010	1

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